2009-06

NPS CubeSat Launcher-lite sequence

Harris, Anthony D.

Monterey, California. Naval Postgraduate School

NAVAL POSTGRADUATE SCHOOL

MONTEREY, CALIFORNIA

THESIS

NPS CUBESAT LAUNCHER-LITE SEQUENCER

by

Anthony D. Harris

June 2009

Thesis Advisor:	James H. Newman
Second Reader:	Daniel Sakoda

Approved for public release; distribution is unlimited

THIS PAGE INTENTIONALLY LEFT BLANK

REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188
Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instruction, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington DC 20503.			
1. AGENCY USE ONLY ***(Leave blank)***	**2. REPORT DATE** June 2009	**3. REPORT TYPE AND DATES COVERED** Master's Thesis	
4. TITLE AND SUBTITLE NPS Cubesat Launcher-Lite Sequencer		**5. FUNDING NUMBERS** **RSPXL**	
6. AUTHOR(S) Harris, Anthony D.			
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Naval Postgraduate School Monterey, CA 93943-5000		**8. PERFORMING ORGANIZATION REPORT NUMBER**	
9. SPONSORING /MONITORING AGENCY NAME(S) AND ADDRESS(ES) National Reconnaissance Office Office of Corporate Communications 14675 Lee Road Chantilly, VA 20151-1715		**10. SPONSORING/MONITORING AGENCY REPORT NUMBER**	
11. SUPPLEMENTARY NOTES The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government.			
12a. DISTRIBUTION / AVAILABILITY STATEMENT Approved for public release; distribution is unlimited		**12b. DISTRIBUTION CODE**	

13. ABSTRACT (maximum 200 words)

The purpose of this thesis is to document my activities related to designing and constructing a flight-like, payload deployment sequencer. The sequencer will be a model of the operational sequencer to be used in the NPS CubeSat Launcher (NPSCuL) project. NPSCuL is being built to address a need for domestic CubeSat launch capability and is designed to launch a significant volume of CubeSats into orbit in a single launch. The NPSCuL will be a secondary payload on U.S. launch vehicles and will be attached to the launch vehicle via the EELV (Evolved Expendable Launch Vehicle) Secondary Payload Adapter (ESPA), or compatible launch vehicle structures. A small version of NPSCuL called NPSCuL-Lite will house CubeSats in up to 8–1x1x3 ("3U") Poly Pico-satellite Orbital Deployers (P-PODs) developed by the California Polytechnic State University (Cal-Poly). The sequencer's function is to issue commands and drive the circuitry to open the P-PODs in the proper sequence. The sequencer may be mounted either externally from the NPSCuL-Lite or internally. Both a functional flight-similar model, and a mass model of the correct size and CG, are required for future testing.

14. SUBJECT TERMS NPSCuL, NPSCuL-Lite, P-POD, Sequencer, Launcher, Launch Vehicle, Microcontroller, Space, Satellite			**15. NUMBER OF PAGES** 192
			16. PRICE CODE
17. SECURITY CLASSIFICATION OF REPORT Unclassified	**18. SECURITY CLASSIFICATION OF THIS PAGE** Unclassified	**19. SECURITY CLASSIFICATION OF ABSTRACT** Unclassified	**20. LIMITATION OF ABSTRACT** UU

NSN 7540-01-280-5500 Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18

THIS PAGE INTENTIONALLY LEFT BLANK

Approved for public release; distribution is unlimited

NPS CUBESAT LAUNCHER-LITE SEQUENCER

Anthony D. Harris
Lieutenant, United States Navy
B.A., San Diego State University, 2005

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN SPACE SYSTEMS OPERATIONS

from the

NAVAL POSTGRADUATE SCHOOL
June 2009

Author: Anthony D. Harris

Approved by: James H. Newman, PhD
Thesis Advisor

Daniel Sakoda, Research Associate
Second Reader

Rudolf Panholzer, PhD
Chairman, Department of Space Systems Academic Group

THIS PAGE INTENTIONALLY LEFT BLANK

ABSTRACT

The purpose of this thesis is to document my activities related to designing and constructing a flight-like, payload deployment sequencer. The sequencer will be a model of the operational sequencer to be used in the NPS CubeSat Launcher (NPSCuL) project. NPSCuL is being built to address a need for domestic CubeSat launch capability and is designed to launch a significant volume of CubeSats into orbit in a single launch. The NPSCuL will be a secondary payload on U.S. launch vehicles and will be attached to the launch vehicle via the EELV (Evolved Expendable Launch Vehicle) Secondary Payload Adapter (ESPA), or compatible launch vehicle structures. A small version of NPSCuL called NPSCuL-Lite will house CubeSats in up to 8–1x1x3 (“3U”) Poly Pico-satellite Orbital Deployers (P-PODs) developed by the California Polytechnic State University (Cal-Poly). The sequencer’s function is to issue commands and drive the circuitry to open the P-PODs in the proper sequence. The sequencer may be mounted either externally from the NPSCuL-Lite or internally. Both a functional flight-similar model, and a mass model of the correct size and CG, are required for future testing.

THIS PAGE INTENTIONALLY LEFT BLANK

TABLE OF CONTENTS

THIS PAGE INTENTIONALLY LEFT BLANK

LIST OF FIGURES

LIST OF TABLES

THIS PAGE INTENTIONALLY LEFT BLANK

LIST OF ACRONYMS AND ABBREVIATIONS

1st LT	First Lieutenant
3D	Three Dimension
A	Amp(s)
ABC	Aft Bulkhead Carrier
BJT	Bipolar Junction Transistor
Cal Poly	California Polytechnic State University
CAD	Computer Aided Design
CDR	Concept Design Review
CDS	CubeSat Design Specification
CG	Center of Gravity
CMOS	Complementary Metal Oxide Semiconductor
CSEWI	California Space Education and Workforce Institute
CubeSat	Cube Satellite
COTS	Commercially Available Off-the-Shelf
DSE	Deployment Subsystem Electronics
DoD	Department of Defense
D-sub	D-subminiature Connector
EELV	Evolved Expendable Launch Vehicle (Atlas and Delta)
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESPA	EELV Secondary Payload Adapter
FRD	Functional Requirements Document

I-DEAS	Original CAD program the team utilized
L41	Launch 41 endorsed by NRO scheduled for August 2010
LEO	Low Earth Orbit
LLC	Limited Liability Company
LV	Launch Vehicle
LTJG	Lieutenant Junior Grade
LT	Lieutenant
LCDR	Lieutenant Commander
mA	Milliamp(s)
MIPS	Multiple Interface Payload Subsystem
MIPS-Lite	The newest, lightest, and NPS compatible MIPS model
MLB	Motorized Lightband
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
msec	Millisecond(s)
NEA	Non-Explosive Actuator
NPS	Naval Postgraduate School
NPSCuL	NPS CubeSat Launcher
NPSCuL-Lite	The newest and lightest version of the NPSCuL
NRO	National Reconnaissance Office
NX-6	A CAD program currently in use by the team
PBASIC	Program used by the basic Stamp microcontroller
PC	Personal Computer
PCB	Printed Circuit Board
PDR	Preliminary Design Review

P-POD-	Poly Pico-Satellite Orbital Deployer
PTB	Primary Test Board
QBX	CubeSat Office
RF	Radio Frequency
RSA	Rideshare Adapter
RTB	Redundant Test Board
SERB	Space Experiment Review Board
SSAG	Space Systems Academic Group
STP	Space Test Program
TBD	To Be Determined
TTL	Transistor to Transistor Logic
ULA	United Launch Alliance
V	Volt(s)
VDC	Direct Current Voltage
VIN	Input Voltage
VTC	Video Teleconference

THIS PAGE INTENTIONALLY LEFT BLANK

ACKNOWLEDGMENTS

The author wants to acknowledge Professor James Newman for his tireless support to the NPSCuL-Lite project. Additionally, he was an integral part of the guidance and mentoring of the author's project. Furthermore, he provided the author with the necessary fundamental knowledge to complete the thesis successfully and in a timely fashion.

The author also wants to thank SSAG faculty members for their valuable support to the successful design and prototyping of the NPSCuL-Lite sequencer. Specifically, the author wants to thank Research Associate Dave Rigmaiden for providing his electrical engineering expertise in creating the electrical circuitry for the sequencer. In addition, the author wants to thank Research Associate Dan Sakoda for providing his CAD modeling and drafting expertise for the initial electronic design of the sequencer.

The author wants to thank the NPSCuL-Lite team. The Project Manager, Christina Hicks, supported the author's efforts throughout the development of the sequencer by displaying tremendous patience and outstanding leadership. Research Associate, Matt Crook, tutored the author in the Rhinoceros CAD modeling program, designed a 3D model of a microcontroller integral to the NPSCuL-Lite demonstration model, and provided valuable support in creating the final designs of the architectural design of the sequencer. The testing and integration member, Adam "Tito" DeJesus, provided necessary guidance in the CAD modeling phase of the sequencer as well as supported "way ahead" efforts.

Finally, the author would like to extend his thanks to Alexander Schulenburg. He selflessly tutored the team in modeling, drafting, and simulation to help bring the NPSCuL-Lite project to the next step. In regard to the author's work, he personally walked the author through step by step on how to create a model through NX-6.

THIS PAGE INTENTIONALLY LEFT BLANK

I. INTRODUCTION

A. NANOSATELLITES AND PICOSATELLITES

1. Nanosatellite and Picosatellite Introduction

Since the 1990s, major satellite manufacturers, government and academic institutions have found great potential in the development of small satellites. These entities have witnessed first hand that small satellites perform to the same standard as many of their predecessors that are multiple times more massive and costly. Nanosatellites can perform missions such as remote sensing, GPS, communications, and other scientific research that traditionally were only performed by larger satellites. Due to their simple structure, advances in technology, the interdependence of several satellite communities, and their inexpensive nature, the proliferation of nanosatellites will increase the intelligence and military capabilities of nations worldwide.

2. Variations of Small Satellites and P-POD Introduction

Since the 1990s, small satellites have gained interest worldwide. They are generally categorized by weight. Small satellites can be categorized as micro (10-100 kg), nano (1-10 kg), or picosatellites (< 1kg) (Zhang et al). CubeSats, 10 cm^3 and 1kg picosatellites, were developed in 1999 as an integrated project between California Polytechnic State University and Stanford University (Schaffner). The purpose of this project is to make smaller and more affordable picosatellites to accomplish civil missions (Schaffner). A P-POD, the common deploying mechanism, enables schools, corporations, and the military worldwide to develop satellites without having to interact directly with the launch providers. The reduced cost and relatively simple and light structure allows for non-traditional communities—such as academic institutions worldwide—to participate in the development and launch of satellites.

3. International Leveraging of Nanosatellites

Nanosatellites can provide satellites with capabilities such as remote sensing, GPS navigation, and communication related missions. The proliferation of nanosatellites have

allowed for many smaller communities to take advantage of these capabilities. Since these capabilities are widespread, certain nations are looking for innovative ways to expand the life and use of nanosatellites. For example, a Japanese institution is creating a way to refuel and recharge a nanosatellite in LEO (Plattard). Specifically, a three dimensional docking mechanism for nanosatellites is being developed by the Laboratory for Space Systems (LSS), Tokyo Institute of Technology (Plattard). The current issue involved in launching nanosatellites to LEO is that their lifespans are too short. LSS is working to resolve that problem through a "mothership-daughtership" satellite framework. The "mothership" is the relatively larger satellite and the "daughtership" is the nanosatellite (Plattard). The mothership performs traditional functions of larger satellite including communicating to ground stations (Plattard). In addition, it provides a mission unique capability of recharging and refueling nanosatellites (Plattard). These nanosatellites are launched from the mothership to perform their specific missions (Plattard). Once the nanosatellites are done with their tasks, they will re-dock with the mothership for fueling (Plattard).

4. Future Visions of Nanosatellites

On a related topic, experts of the nanosatellite community project that one day nanosatellites will be flying in formation, mass produced, and launched for missions. One source envisions a spherical constellation of several thousand nanosatellites to satisfy future civilian and military needs (Dwyer). Other ideas include using thousands of nanosatellites to be deployed from a dispenser to provide a continuous planar ring of satellites for communication purposes (Dwyer). Gerard Dwyer, the author of this article, estimates that 400 nanosatellites can provide 95% Earth coverage for remote sensing, navigation, and communication missions (Dwyer). He also mentions that this concept would be especially appealing to the military to have a constellation of inexpensive and relatively simplistic satellites.

5. COTS Technology Availability for Nanosatellites

COTS technology and launch vehicle availability have grown in recent years worldwide. This may pose a threat to the U.S. and friendly forces as other potential threat

countries can utilize these capabilities. THNS_1 is the first nanosatellite (10 kg) under development at Tsinghua Space Center, China (Zhang et al).

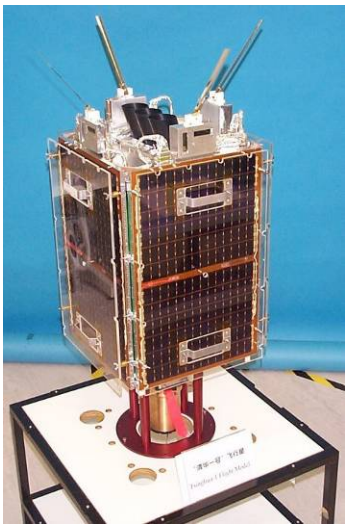


Figure 1. Tsinghua-1 Nanosatellite (From http://centaur.sstl.co.uk/SSHP/pix/Tsinghua-1.jpg)

It was successfully launched into space April 19, 2004 ("China Develops First Nano-Satellite"). It carries four experimental payloads: a GPS receiver, CMOS camera, micro inertia measurement unit (MIMU), and a micro propulsion system (Zhang et al). On this satellite, the GPS receiver system is based off of COTS technology manufactured by Mitel Semiconductor (Zhang et al). With the launch of a nanosatellite and use of COTS technology the Chinese have shown the world that it is capable of competing with the U.S. in the small satellite arena. Furthermore, the use of COTS technology shows that they have ample resources to proliferate nanosatellites for their own national interests.

6. Launch Availability for Nanosatellites

In regard to launch availability, a new launch facility exists in India which has provided launch capability to several international nanosatellite manufacturers. On April 28, 2009, Indian Space Research Organization launched 8 nanosatellites on the Polar Satellite Launch Vehicle, PSLV-C9 for international customers into a 637 km sun-synchronous orbit ("India's PSLV Successfully Launches Ten Satellites").

Figure 2. PSLV Launch (From www.gufaratiblogger.com/uploads/PSLV-C11%20LiftOff.jpg)

Canada, Denmark, Japan, Germany, Netherlands, and Japan each produced nanosatellites for this launch ("India's PSLV Successfully Launches Ten Satellites"). Coincidentally, University of Toronto Institute for Aerospace Studies/Space Flight Laboratory (UTIAS/SFL) negotiated with Antrix Corporation for launch of 6 of the 8 nanosatellites ("Low-Cost Launch Service"). What this information suggests is that several countries—including potential adversaries—are involved with nanosatellite technology and rideshare programs to accomplish their unique missions. Once again, these missions may be potentially harmful to U.S. national security. The fact that space is becoming available to almost everyone now may prove to be costly to the U.S. and its allies.

7. International Cost Comparison of a Nanosatellite

Israel Nanosatellite Association (INSA) plans to launch its first nanosatellite in mid-2009 ("Israel Plans Launch of Nano-Satellites as Low Cost Alternative to GPS Satellites"). The purpose of this launch is to demonstrate the feasibility of using nanosatellites as GPS systems rather than the older GPS platform in order to reduce GPS costs ("Israel Plans Launch of Nano-Satellites as Low Cost Alternative to GPS Satellites"). Each nanosatellite would cost about $150,000 ("Israel Plans Launch of Nano-Satellites as Low Cost Alternative to GPS Satellites"). This is one-hundredth of the cost of a standard LEO satellite that costs $15 million ("Israel Plans Launch of Nano-Satellites

as Low Cost Alternative to GPS Satellites"). A nanosatellite or a system of nanosatellites will provide the same capability with lower cost. Given this information, it is obvious that the capability versus cost ratio of nanosatellites is excellent relative to older satellite platforms. Israel plans to assemble constellations of these nano-platforms in space. The satellites will be launched from India's Satish Dhawan Space Center ("Israel Plans Launch of Nano-Satellites as Low Cost Alternative to GPS Satellites").

8. Potential Threats

China and India pose some of the greatest threats to U.S. national security. With nanosatellite technology within grasp, they could potentially exploit this technology to gain intelligence or to put the U.S. in a vulnerable position. In 2002, the Chinese created the 10 kg Tsinghua nanosatellite (Xiong). Their onboard computer subsystem manages satellite operations, performs altitude control and processes science data (Xiong). The payload on this satellite is a micro Multi-Spectral Earth Imaging system with three on-chip CMOS CCD cameras on it (Xiong). The cameras can sample with a ground resolution of 250 meters in 3 spectral bands with a 75 km field of view (Xiong). With this sort of capability, China could potentially image key target areas, gain crippling intelligence to U.S. national security, form and execute a plan to weaken U.S. defenses.

Another potential threat to the U.S. is India and its launch facilities. As mentioned before, India has already displayed the capability of launching full and nano-sized satellites into space. Furthermore, they have also displayed the capability of integrating with foreign nanosatellite technology by launching the PSLV-C9 launch and the prospective Israeli GPS receiver nanosatellite launch. This gives U.S. adversaries a leveraging point to launch their satellites into space. For instance, China, being a threat to the U.S., could capitalize on India's space facility to perform specific missions to increase the vulnerability of the U.S. and its allies via space.

9. Nano and Picosatellite Conclusion

As mentioned before, there are current visions of mass producing and launching of nanosatellites to form LEO constellations for civil and military missions. Smaller nations will enjoy the benefits of this mass production as the world becomes more

interdependent. In addition, small nations currently have the capability to benefit from nanosatellite technology. Once again, Israel is capitalizing on this technology by planning a two-satellite flight demonstration in 2009 of a GPS navigation system to replace the obsolete traditional satellites they are currently employing.

Other countries are making their appearances now in the satellite community and may continue to emerge as a global space power in the future. In 1997, Malaysia launched the Tiung-Sat microsatellite into orbit on a DNEPR launch vehicle ("Surrey Missions: TiungSat-1"). They intend to use microsatellites to enhance small and intermediate scale agricultural productivity ("Surrey Missions: TiungSat-1"). This is achieved by gathering information on local climate, soil characteristic identifications, and other communication systems enabled by microsatellites ("Surrey Missions: TiungSat-1"). Other benefits include: reducing transportation costs by optimizing land and sea routes, and establishing warning systems ("Surrey Missions: TiungSat-1"). In the future and with advancing technology, countries like Malaysia could employ the same satellite functionality on satellites orders of magnitude smaller than their predecessors.

B. NPSCUL/NPSCUL-LITE PROGRAM HISTORY

1. NPSCuL

The Naval Postgraduate School Space Systems Academic Group (SSAG) has designed and constructed small satellites for two decades (Crook). The group has been involved with several space related projects. Two of the more notable projects are the first NPS satellite, the Petite Amateur Navy Satellite (PANSAT), and the NPSAT1 satellite (Crook).

Unlike PANSAT, NPSAT1 is not designed to be launched from the space shuttle. It was intended to be launched on another space launch vehicle called an evolved expendable launch vehicle (EELV) as a secondary payload using the EELV Secondary Payload Adapter (Crook).

The EELV is the current primary method of transportation for many small and low priority payloads to get to orbit. Traditionally, there has been excess capacity on these EELVs. Specifically, the amount of wasted space equates to hundreds or thousands

of kilograms of unused, excess capacity on these vehicles (Buckley). Considering the potential benefits, the small satellite community has endeavored to utilize this excess capacity to launch secondary payloads into space.

Certain mechanisms were constructed to interface secondary payloads to EELVs. The EELV secondary payload adapter (ESPA) ring is that interfacing adapter. It is an adapter that can hold and attach 6 secondary payloads to the EELV (Crook).

Figure 3. ESPA Ring (From Crook)

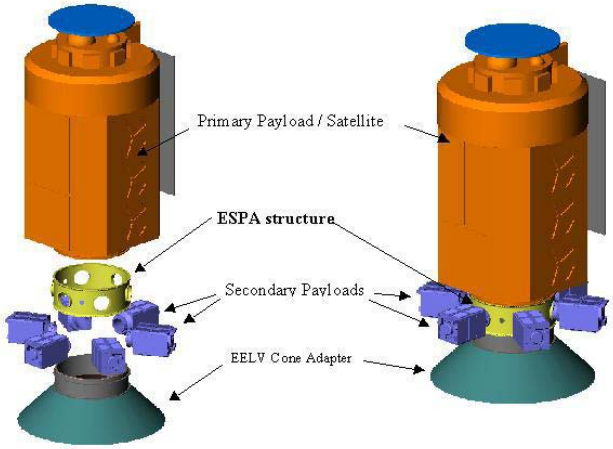


Figure 4. Conceptual ESPA Integration (From Crook)

For various reasons, NPSAT1 could not make the first ESPA launch, STP-1, in March 2007 (Crook). However, NPS had to produce a mass simulator to provide the same inertial properties that the launch provider planned for in the mass and center of gravity (CG) analysis of the launch vehicle. After this occurred, the SSAG realized that small satellites have a higher risk than larger satellites of missing launches. NPS saw an opportunity to allow other small satellite programs to catch future flights. However, it is not as simple as talking to the launch provider and proposing any secondary payload to fill any available slots. In fact, ESPA payloads cannot be easily substituted with other

payloads because the inertial characteristics must match from payload to payload. Consequently, Dr. Rudolf Panholzer and Dr. Jim Newman, members of the NPS SSAG, theorized a mass simulator that could allow for a short notice reconfiguration of mass and CG characteristics that would also match other secondary payload inertial properties (Crook 08).

The SSAG faculty thereafter refined their concept into something that could fit into a slot in the ESPA ring (Crook). They decided that a CubeSat launcher would fit appropriately. A CubeSat launcher would effectively utilize the ESPA ring volume and mass. In addition, it would also allow for the launch of an unprecedented amount of CubeSats into orbit in a short time period. The concept solidified into a project called the NPS CubeSat launcher (NPSCuL) project (Crook).

Figure 5. The "D-Advanced" Structure Final NPSCuL Design (From Crook)

2. NPSCuL-Lite

During a conference in Logan, UT in August 2008, SSAG faculty members and interested students at NPS coordinated with key figures. The NPS team met with the California Polytechnic State University (Cal Poly), Space Test Program (STP), and CubeSat office (QBX) representatives to discuss actual funding and procurement of the NPSCuL. These series of meetings could be considered as the birth of the NPS CubeSat Launcher Light Version (NPSCuL-Lite) project and team.

Several weeks later, the newly formed NPSCuL-Lite team began holding weekly meetings, teleconferences with other interested and related entities. As a result of the series of discussions with external partners, the concept of the NPSCuL-Lite materialized on paper. Through the several interactive discussions, it was decided that the NPSCuL-Lite will have a lower mass and a shorter Z-directional height in respect to the original NPSCuL. Furthermore, its P-POD carrying structure will be altered into a more streamlined structure that meets United Launch Alliance (ULA) envelope requirements. Finally, instead of carrying P-PODs external to the structure, the NPSCuL-Lite's design is modified to enclose all the P-PODs.

A drawback to the "Lite" design is that it cannot support the CubeSat carrying capability that the NPSCuL could foster. With larger P-PODs, the NPSCuL could effectively carry and launch up to fifty CubeSats into orbit. The NPSCuL-Lite can hold only 24 CubeSats in eight 3-U Cal Poly P-PODS.

C. SEQUENCER INTRODUCTION

1. NPSCuL-Lite Requirement for the Sequencer

During the meetings in Logan, UT the topic of a sequencer device came up. A sequencer is an electronic device that contains the logic, electrical hardware, and interfacing capability with the launch vehicle and P-PODs to open the P-POD doors in a certain timed sequence. It was mentioned that an outside source would procure a sequencer module for the NPSCuL-Lite. In addition, there was a chance that the NPSCuL-Lite project would have received additional funding to acquire a tested and qualified sequencer for the project. As the project evolved, the chances of either of those situations reduced.

All in all, the NPSCuL-Lite project still requires a sequencer to perform its mission. It still needs a device that is capable of being the electrical interface between the launch vehicle, NPSCuL-Lite chassis, and the P-PODs. On that note, the NPSCuL-Lite team learned that Design Net Engineering was building a sequencer that could

possibly be used to deploy the P-PODs on an NPSCuL-Lite mission. The team decided to work with Design Net Engineering to create a space qualified sequencer specifically for the NPSCuL-Lite structure.

Initially, the school did not have the funds to purchase Design-Net's sequencer. Additionally, one of the risks that the team had to endure was a potential reality that the team may not ever have the funds to purchase the sequencer. On that note, the small satellite community manages many risks. One of those risks is having insufficient funds to support a small satellite program. Therefore, in an effort to mitigate this risk, the NPSCuL-Lite team decided to design and construct an in-house functional prototype sequencer for the purposes of testing and supporting the efforts of further design projects related to the overall NPSCuL-Lite project.

D. OBJECTIVES

1. Purpose

The purpose of this thesis is to document the activities related to designing and constructing a flight-like, payload deployment sequencer. This flight-like sequencer will not be the actual sequencer that will be attached to the NPSCuL-Lite for the L41 launch in 2010. The actual sequencer that is expected to be attached to the NPSCuL-Lite for the L41 launch is the Design Net Multiple Interface Payload Subsystem (MIPS) sequencer. The flight-like sequencer that the author is creating will serve as a prototype of the Design Net payload deployment sequencer. Furthermore, the flight-like model will serve as a device to facilitate student education and the overall testing and development of the NPSCuL-Lite project.

NPSCuL is being built to address a need for domestic CubeSat launch capability and is designed to launch a significant volume of CubeSats into orbit in a single launch. The NPSCuL will be a secondary payload on U. S. launch vehicles and will be attached to the launch vehicle via the EELV Secondary Payload Adapter (ESPA), or compatible launch vehicle structures. A small version of NPSCuL called NPSCuL-Lite will house CubeSats in up to 8 - 1x1x3 ("3U") Poly Pico-satellite Orbital Deployers (P-PODs) developed by the California Polytechnic State University (Cal-Poly). The sequencer's

function is to issue commands and drive the circuitry to open the P-PODs in the proper sequence. The sequencer may be mounted either externally from the NPSCuL-Lite or internally. Finally, both a functional, flight-similar model and a mass model of the correct size and CG are required for testing.

2. Objectives the Thesis Aims to Accomplish

- ***The thesis will document the process of developing and designing a prototype sequencer including interactions with other third parties related to this thesis.***
- ***The thesis will define necessary performance requirements that the NPSCuL-Lite sequencer must satisfy for testing***
- ***The thesis will define the purpose of having a flight-similar model and a mass model of the sequencer.***
- ***The thesis will explain how the internal circuitry, command logic, and the opening sequence operate.***
- ***The thesis will illustrate any other necessary modifications that have to be implemented in order to ensure the successful integration of the sequencer with the NPSCuL-Lite.***
- ***The thesis will document preliminary thermal-vacuum testing done on the sequencer testing board***

3. Objectives Conclusion

a. A Brief Guide to the Overall Thesis

The author would like to note that the NPSCuL-Lite project is an on-going project. The schedules, budgets, processes, testing, and analyses that will be documented in this thesis are dealing with present issues during the time this thesis is written. In addition, the author would like to mention that in the following text the author will occasionally refer to third persons as the generic word “he.” The author would prefer that the reader interprets this to include both genders.

The purpose behind the introduction is to introduce elements of the small satellite community and how it relates to the projects performed at NPS. Moreover, the intent

behind the introduction is to validate and solidify the concept of the NPSCuL-Lite project including the prototype sequencer. The next stage of the thesis development aims to move away from the broad overall view of small satellites, the geopolitical market of these satellites, and the CubeSat community.

Unlike the introduction, the next several chapters of this thesis will attempt to delve into the NPSCuL-Lite project and its related components. Thus, the reader will get detailed insight in how the global small satellite market spurs the development and innovation of newer small satellite innovations within the smallest of institutions. The NPSCuL-Lite Prototype Sequencer is one of these innovations that were made possible by the relatively recent global proliferation of small satellite technology.

b. A Brief Guide to the Following Chapters

The second chapter includes overall timelines, budgets of the NPSCuL and NPSCuL-Lite, and finally, timelines and budgets of all elements relating to the NPSCuL-Lite Prototype Sequencer. The purpose of this is to bring awareness to the reader about the general timeframe, associated project expenditures, and a general understanding of the working and refinement process of key members associated with the prototype sequencer project.

The third chapter embellishes the finer details concerning the mechanical interface of the prototype. This chapter includes the learning process of computer software to develop proper models, cooperative discussions with external entities, models from external entities, errors during the external chassis development, the resultant products of labor, and the effects induced on the rest of the team.

The fourth chapter amplifies detailed characteristics of the prototype electrical interface. The chapter discusses preliminary conceptual models and diagrams, the development process of the primary test board, the test board electrical process, and a glance at all the internal components of the test board.

The fifth chapter elaborates on the thermal-vacuum procedure administered for the project. It illuminates details concerning the thought process behind

the test, the reference manual that is the standard of the test, the three different test cycles and purposes, data retrieved from testing, and troubleshooting methodologies.

The conclusion chapter wraps up the entire project and offers suggestions for future work. Any concluding remarks in respect to the project are documented here. In addition, the author will provide recommendations for further thesis opportunities for future students.

Finally the last segment of this thesis is the appendices. This section includes a preliminary functional requirements document of the prototype and a preliminary thermal testing procedure. These documents serve as a more detailed look at the inner workings of the prototype sequencer.

THIS PAGE INTENTIONALLY LEFT BLANK

II. TIMELINES AND BUDGETS

The following chapter discusses the timeline and budget of the sequencer produced by Design Net and the prototype sequencer for the NPSCuL-Lite project. Information concerning the timeline, development, and budget of the overall project and integration and testing will be discussed in other team members' theses. Specifically, the overall NPSCuL-Lite project timeline and budget is discussed by Christina Hicks' thesis, "NPS CubeSat Launcher (NPSCuL-Lite) Program Management." The integration and testing timeline and budget is elaborated in Adam DeJesus' thesis, "Integration and Environmental Qualification Testing of the Spacecraft Structures in Support of the NPS CubeSat Launcher Program."

A. MIPS TIMELINE AND COST

1. Design Net Timeline October through January 2008–2009

Currently, Design Net is developing the multi-interface payload system (MIPS) model to serve as a sequencer for the team's project. The MIPS evolved from the deployer subsystem electronics (DSE) developed for small Falcon class launch vehicles (Murphy). Design Net was first introduced to the current NPSCul-Lite student team during small satellite convention in 2008. The principal investigator and the author formed a working relationship with the company shortly thereafter.

The company issued the initial product specification draft in late October. The document delivers an introductory look of the scope, electrical and mechanical requirements. This draft served as the working document that catalyzed the initial concept creation of the NPSCuL-Lite sequencer.

In December, Design Net attended the Denver PDR and released further detailed specifications of the MIPS. During the PDR, Gerald Murphy, the chief engineer for the MIPS, brought up key issues that would determine the final design of the MIPS. Among some of the issues were MIPS capabilities based on electromagnetic interference protection, P-POD door sensors, and telemetry. In addition, during the December and January time frame, Design Net released MIPS charts, envelope drawings, and inertial

properties. With this information, the author was armed with all the information to create a CAD model that had the proper dimension attributes as the MIPS.

2. Design Net Timeline March 2009 through L41 Launch

In March, Design Net released the MIPS inertial properties, the final product specification document, and delivered a price estimate for the MIPS. The release of the MIPS inertial properties allowed the author to physically construct a mass model of the MIPS with the proper dimension and CG attributes. The final product specification gave the author all the necessary information to create the prototype sequencer's functional requirement document, it allowed for electrical components to be ordered, and it allowed for actual circuitry to be created. Furthermore, this guide was the final piece necessary to integrate the mechanical and electrical elements of the prototype into one complete unit.

From April until the L41 launch, Design Net is responsible for many deliverables in a relatively short time period. In April, a conference was held between Design Net,QBX, and NPS to discuss payments delivered to Design Net. After the conference, Mr. Murphy requested to use the school's testing facilities in May to qualify the MIPS box as well as other Design Net projects. Mr. Murphy also stated that his team would produce an engineering unit by late October. Finally, he stated that in early 2010 Design Net would deliver a MIPS flight unit for the L41 launch later that year.

3. Ecliptic

Originally, Design Net was the sole provider of the NPSCuL-Lite sequencer. As such, the NPSCuL-Lite team decided originally to make a prototype sequencer that has the same form, fit, and function of the Design Net's device. Later in the project, QBX considered another device from a company called Ecliptic Enterprises Incorporated. This company states they can deliver a flight qualified sequencer for about the cost of the MIPS in less time. They state they can deliver this unit in September 2009. Even though QBX considered this different manufacturer, the team still pressed forward with the same model that Design Net produced for the team. After all, actual aluminum had been machined, bolt hole footprints were already established, several man-hours and funds had been spent designing the structure that was created.

The following table summarizes the schedule of the MIPS from concept creation to the L41 launch.

	Task Name	Duration	Start	Finish	Predecessors	Resource Names
1	**MIPS**	**298 days**	**6-Aug-08**	**24-Sep-09**		Design Net Engineering LLC
2	**MIPS Proposal**	**2 days**	**6-Aug-08**	**7-Aug-08**		Design Net Engineering LLC
3	Initial Released MIPS Product Specification	1 day	31-Oct-08	31-Oct-08		Design Net Engineering LLC
4	ULA PDR	1 day	18-Dec-08	18-Dec-08		Design Net Engineering LLC
5	MIPS Charts Release	1 day	22-Dec-08	22-Dec-08	3	Design Net Engineering LLC
6	MIPS Envelope Drawing	1 day	26-Jan-09	26-Jan-09	3	Design Net Engineering LLC
7	MIPS Inertial Properties Release	1 day	3-Mar-09	3-Mar-09	3	Design Net Engineering LLC
8	Final Released MIPS Product Specification	1 day	22-Mar-09	22-Mar-09	3	Design Net Engineering LLC
9	Delivery of Price Estimate	1 day	27-Mar-09	27-Mar-09		Design Net Engineering LLC
10	Initial Scheduled Payment and Discussion to Design Net	1 day	20-Apr-09	20-Apr-09	9	Design Net Engineering LLC
11	Design Net Vibration Test	1 day	10-May-09	10-May-09	9	Design Net Engineering LLC
12	Delivery of Ecliptic Sequencer Flight Unit	1 day	1-Sep-09	1-Sep-09		Design Net Engineering LLC
13	Delivery of MIPS Engineering Unit	1 day	31-Oct-09	31-Oct-09	11	Design Net Engineering LLC
14	Delivery of MIPS Flight Unit	1 day	1-Mar-10	1-Mar-10	13	Design Net Engineering LLC
15	L41 Launch	1 day	1-Aug-10	1-Aug-10		Design Net Engineering LLC

Table 1. MIPS Schedule from Conception to L41 Launch

B. NPSCUL-LITE PROTOTYPE SEQUENCER TIMELINE AND COST

1. Independent Study Background

The timeline of the NPSCuL-Lite sequencer actually starts two months before the conception of the NPSCuL-Lite project. The author started out with an independent study course for the summer quarter of 2008. The purpose of this study was to have one-on-one instruction on a particular research topic that the SSAG faculty were particularly interested in. At this time, Mr. Crook was still in charge of the original NPSCuL project and still needed associates to facilitate the design process of the project. Specifically, he was looking for a relief for the program manager job, a testing and integration individual, a structures expert, and a member to handle the electrical interface of the NPSCuL project. The author decided to fill the electrical interface slot of the NPSCuL project.

On that note, the author signed up for an independent study in July dealing with understanding and leveraging the capabilities of a microcontroller for the NPSCuL project. In early July, the author was given an introduction to the lab environment. This included walking through the SSAG lab facilities at NPS, meeting the several engineering professionals that the author would end up working with in the future, seeing the several materials the author would have to work with, and getting assigned a desk to start work. The independent study work included multi-disciplinary research that provided the necessary foundation for the prototype sequencer work. Some of these elements included research in microcontroller products, microcontroller programming, Rhinoceros CAD programming, wiring, soldering, and utilizing 3D printing resources. After this background research, the author officially began his research on the prototype sequencer.

2. NPSCuL-Lite Prototype Sequencer Timeline October-January 2008-2009

In October and November, the preliminary designs of the sequencer were created. Design Net issued its initial product specification document for the MIPS in late October. This document provided the proper foundation to start creating a CAD model in I-DEAS. Coincidentally, the author was taking a spacecraft systems design class that necessitated

the use of I-DEAS to create a thermal simulation model. The student learned how to model, apply finite element analysis, and simulation. This introductory look at I-DEAS provided the author a good starting point to do more advanced work with I-DEAS involving the prototype. Consequently, the prototype sequencer mass model was constructed through I-DEAS.

Additionally, during the same timeframe, electrical schematics were created to provide a conceptual elaboration of the prototype's electrical interface. The author produced a Microsoft Visio model to explain the big picture functions of the sequencer. This document facilitated the team's understanding of what the sequencer was going to accomplish. In addition, it provided a preliminary look at the complexity of work that would be required. The document also provided some understanding on the variety of parts that would need to be tested and purchased.

In December, a pivotal event occurred that provided more clarity to the project requirements. The ULA PDR occurred in mid December. During the PDR, the hosts provided documentation that delineated the specifics of all of the associated systems and subsystems of the L41 launch. Furthermore, this document provided detailed information about the Design Net MIPS and how it would interface with the NPSCuL-Lite secondary payload. This document provided great clarity in what kind of requirements need to be met in order to create a flight qualified sequencer. On that note, the document gave the author some insight on what was possible to accomplish in the remaining months of thesis work.

The following table summarizes the prototype timeline between October to December 2008.

	Task Name	Duration	Start	Finish	Prede-cessors	Resource Names
1	**NPSCuL-Lite Prototype Sequencer**	**353 days**	**1-Jul-08**	**19-Jun-09**		
2	**NPSCuL-Lite Proposal**	**2 days**	**6-Aug-08**	**7-Aug-08**		NPS Team
3	Conference with THE SPONSOR, STP, and Cal Poly	1 day	15-Oct-08	15-Oct-08		NPS Team
4	Initial Released MIPS Product Specification	1 day	31-Oct-08	31-Oct-08		Design Net
5	I-DEAS Training	60 days	1-Nov-08	31-Dec-08		NPS Team
6	AE 4831 Modeling , Finite Element Analysis, Simulation	41 days	1-Nov-08	10-Dec-08		
7	Prototype Sequencer Mass Model Dimension Model	31 days	1-Dec-08	31-Dec-08		
8	Microsoft Visio Conceptual Electrical Design	16 days	15-Nov-08	1-Dec-083		
9	ULA PDR	1 day	18-Dec-08	18-Dec-08		ULA, NPS Team

Table 2. Timeline of the Prototype from October to December 2008

3. NPSCuL-Lite Prototype Sequencer Timeline December – April 2009

In late December, Design Net released the MIPS charts that provided further detailed information about the MIPS that the previous conferences and documents did not deliver. At this time, Mr. Justin Jordan joined the team as the electrical interface technician for the prototype sequencer. He spent the first few weeks learning about the project, honing his skills in Stamp programming, and gathering materials to conduct further electrical work. In January he ordered electrical components for testing. The purpose behind this expenditure was to examine which components and circuit setups would work best for the final PCB design.

Meanwhile, the MIPS envelope drawing arrived from Design Net. This drawing gave the final proper dimensions to allow for the accurate modeling of the prototype sequencer. The next logical step was to order the material and screws respectively from Hadco Metal Trading Company, LLC and B & B Socket Products, Incorporated. With the material in hand, all that was needed was to model the prototype, draft the associated drawings, and print the 3D model for a fit check.

In early March, the author collaborated with 1st LT Alex Schulenburg, another new student who joined the team. Mr. Schulenburg provided the author with training in a different CAD modeling program called NX-6. The students working on the team found

it rather difficult to use I-DEAS for advanced modeling. NX-6 became the accepted solution for the team. In less than a week, the author and Schulenburg created a mass simulator sequencer with associated drawings. At this point, the author was ready for physical construction of the model. The plastic model was printed in a day. And, the machined model was not finished for 51 days due to the tremendous workload that the machinist, Mr. Harrell had undertaken.

In late March, the prototype functional requirements document was created, modifications occurred, and more collaboration continued. This document has changed several times due to the updated requirements of Design Net and the mission. During this time, the team realized a significant mistake with the prototype sequencer. The hole footprint of the plastic and machine models were not correct and did not match the holes of the appropriate face of the NPSCuL-Lite. This required more allotted time for both models to be modified to accurately reflect these changes. Taking into consideration these two occurrences, the author was able to move forward and create the final prototype model in April. There were a few revisions to this model due to expert advice and incorrect assumptions. However, no significant errors were made in the development of the final prototype model.

More extensive collaborative design efforts continued in March and April. During the previous months, the author was gaining progressively more insight on the requirements that were passed down from Design Net. With these requirements, the author was able to refine a set of local requirements that would be applied to the prototype sequencer. Then, it was necessary to work together with Mr. Jordan to create the proper form, fit, and function of the prototype sequencer. Several meetings took place to solidify the mechanical and electrical designs, answer any questions, and provide the proper path forward.

Currently, the plastic model has minor discrepancies that need to be addressed. Once that occurs, drawings can be drafted, and the final external chassis can be machined. In regard to Mr. Jordan, he is currently continuing work on programming, electrical component testing, and ordering materials for the final construction and integration of electrical and mechanical parts of the prototype sequencer.

The following table depicts the prototype timeline between December 2008 and May 2009.

	Task Name	Duration	Start	Finish	Predecessors	Resource Names
1	**NPSCuL-Lite Prototype Sequencer**	**353 days**	**1-Jul-08**	**19-Jun-09**		
2	**NPSCuL-Lite Proposal**	**2 days**	**6-Aug-08**	**7-Aug-08**		NPS Team
3	ULA PDR	1 day	18-Dec-08	18-Dec-08		ULA, NPS Team
4	MIPS Charts Release	1 day	22-Dec-08	22-Dec-08		Design Net
5	Electrical Components Ordered for Testing	1 day	15-Jan-09	15-Jan-09		Justin Jordan
6	MIPS Envelope Drawing	1 day	26-Jan-09	26-Jan-09		Design Net
7	Aluminum and Screws Order and Delivery	15 days	1-Feb-09	14-Feb-09	6	NPS Team
8	MIPS Inertial Properties Release	1 day	3-Mar-09	3-Mar-09		Design Net
9	NX-6 Work for Prototype Mass Model	1 day	4-Mar-09	4-Mar-09	6,9	Alex Schulenburg
10	Prototype CAD with Proper CG and Dimension	1 day	4-Mar-09	4-Mar-09		Alex Schulenburg
11	Completed Drawings	5 days	5-Mar-09	9-Mar-09		
12	3D Printed Prototype Mass Model	1 day	5-Mar-09	5-Mar-09	9	Dan Sakoda
13	Prototype Mass Model Machining Process and Delivery	51 days	9-Mar-09	20-Apr-09	13	Glenn Harrell
14	Prototype Functional Requirements Document Version I	9 days	1-Mar-09	9-Mar-09	4,8	
15	NPS hosted Conference with THE SPONSOR, STP, and Cal Poly	1 day	10-Mar-09	10-Mar-09		NPS Team
16	Final Released MIPS Product Specification	1 day	22-Mar-09	22-Mar-09		Design Net
17	Prototype Functional Requirements Document Version II	7 days	22-Mar-09	28-Mar-09	14,16	
18	NX-6 Work for Final Prototype Model	42 days	22-Mar-09	2-May-09	9,16	
19	Prototype CAD Model Version I	13 days	22-Mar-09	3-Apr-09		
20	Prototype CAD Model Version II	15 days	3-Apr-09	17-Apr-09		
21	Completed Drawings	2 days	1-May-09	2-May-09		
22	Delivery of Price Estimate	1 day	27-Mar-09	27-Mar-09		Design Net
23	Initial Scheduled Payment and Discussion to Design Net	1 day	20-Apr-09	20-Apr-09		THE SPONSOR, Design Net
24	3D Printed Prototype Final Model	1 day	4-May-09	4-May-09	18	Design Net
25	Final Prototype Model Machining Process and Delivery	14 days	10-May-09	23-May-09	16	Glenn Harrell

Table 3. Timeline of the Prototype from December 2008 to May 2009

4. NPSCuL-Lite Prototype Sequencer Timeline May 2009 – L41 Launch

Several tasks still need to be done before the launch occurs in August 2010. It is unlikely that the NPSCuL-Lite sequencer will undergo the process of space qualification in the next year. Therefore, the author does not include specific times for certain activities to take place. However, it is still desired to follow a similar timeline for educational purposes. Therefore, the next student could possibly work on some of these tasks as a future thesis project. First, the integration of the mechanical and electrical components of the prototype sequencer still needs to be done. Next, thermal-vacuum and vibration testing needs to be completed. This process can take anywhere from a few weeks to a few months depending on resource availability. Finally, once all the testing is completed, the device needs to be delivered to the proper launch authorities for integration and launch. Typically, this delivery occurs six months prior to launch.

The following table depicts a proposed prototype timeline from May 2009 to August 2010.

	Task Name	Duration	Start	Finish	Prede-cessors	Resource Names
1	**NPSCuL-Lite Prototype Sequencer**	**353 days**	**1-Jul-08**	**19-Jun-09**		
2	**NPSCuL-Lite Proposal**	**2 days**	**6-Aug-08**	**7-Aug-08**		NPS Team
3	Design Net Vibration Test	1 day	10-May-09	10-May-09		Design Net
4	Integration of Electrical/Mechanical Parts of Final Prototype	2 days	24-May-09	25-May-09		Justin Jordan
5	Testing of Completed Prototype Sequencer	7 days	26-May-09	1-Jun-09		David Rigmaiden
6	Thermal and Vacuum	3 days	26-May-09	28-May-09		David Rigmaiden
7	Vibration	4 days	28-May-09	1-Jun-09		David Rigmaiden
8	Pass Down to Next Student	7 days	2-Jun-09	9-Jun-09		
9	Delivery of Ecliptic Sequencer Flight Unit	1 day	1-Sep-09	1-Sep-09		Ecliptic Enterprise
10	Delivery of MIPS Engineering Unit	1 day	31-Oct-09	31-Oct-09		Design Net
11	Delivery of MIPS Flight Unit	1 day	1-Mar-10	1-Mar-10		Design Net
12	L41 Launch	1 day	1-Aug-10	1-Aug-10		ULA, THE SPONSOR

Table 4. Timeline of the Prototype from May 2009 to August 2010

5. NPSCuL-Lite Prototype Sequencer Expenditures

a. Components Ordered for Testing

In respect to the NPSCuL-Lite project as a whole, minimal funds were spent on the prototype sequencer. The expenditures of the mechanical components approximately equated to the expenditures of the electrical components. However, the budget displayed in the table below does not take personnel salaries into consideration. If salaries were taken into consideration, the expenses would have been significantly higher. The budget does not reflect the salaries of the principal investigator and other overseeing officials in the department that make this project possible. In regard to the mechanical portion of the project, the budget does not take into consideration the salaries of the machinist, staff engineers, or other students who provided input on the mechanical interface. In respect to the electrical interface, the budget does not take into account the salaries of Mr. Justin Jordan's internship, engineering staff, and the salaries of other students who provided input.

Below is a table illustrating the associated costs of mechanical and electrical components used to create the prototype sequencer.

Qty	Units	Description, Manufacture, Model #, Part#, Catalog#	Price	TOTAL
		Mechanical Components		
25	1	92423A511, 10-32 x 3/4" Passivated A286 Super Alloy Socket Head Cap Screw*	$2.26	$56.50
2	1	P614T651 4.00" x 8.00" x 12.5" Aluminum Plate 6061 T651 (Foreign Material)*	$255.82	$511.64
		Total		$568.14
		Electrical Components		
3	1	Printed Circuit Board, SSAG-PCB0001 REV. A	$101.33	$303.99
1		Shipping & Handling	$16.00	$16.00
3	1	IC REG SIMPLE SWITCHER TO-263-7, National Semiconductor, Part# LM2678S- 12/NOPB, Catalog# LM2678S-12-ND,	$6.24	$18.72
3	1	INDUCTOR 33UH 5A 260KHZ KLIPMNT, Pulse, Part# P0849NL, Catalog# 553-1122-ND	$3.09	$9.27
3	1	CAP TANT LOESR 100UF 16V 10% SMD, AVX Corporation, Part# TPSD107K016R0125, Catalog# 478-1778-1-ND	$4.20	$12.60
9	1	CAP TANT 15UF 50V 20% SMD, Vishay/Sprague, Par# 594D156X0050R2T, Catalog# 718-1008-1-ND	$7.55	$67.95
3	1	DIODE SCHOTTKY 5A 40V SMC, Vishay/General Semiconductor, Part# SSC54-E3/57T, Catalog# SSC54-E3/57TGICT-ND	$0.54	$1.62
6	1	TRANSISTOR NPN 75V 0.6A TO-18, STMicroelectronics, Part# 2N2222A, Catalog# 497-2598-ND	$1.12	$6.72
6	1	IC INDUCTIVE LOAD DRVR 14V SOT23, On Semiconductor, Part# NUD3112LT1G, Catalog# NUD3112LT1GOSCT-ND	$0.60	$3.60
6	1	IC MOSFET DRV DUAL NONINV 8-SOIC, Maxim Integrated Products, Part# MAX4427ESA+, Catalog# MAX4427ESA+-ND	$4.03	$24.18
6	1	RELAY GP SPST-NO 10A 12VDC, Tyco electronics, Part# OJE-SH-112HM,000, Catalog# PB876-ND	$1.15	$6.90
6	1	RELAY PWR HI-CAP 200MW 12VDC PCB, Panasonic Electric Works, Part# JQ1AP-12V-F, Catalog# 255-2071-ND	$3.58	$21.48
6	1	RELAY PWR SPST 16A 12VDC PCB, Omron Electronics Inc-ECB Div, Catalog# Z2580-ND	$2.81	$16.86
6	1	RELAY AUTO 10A 12VDC SEALED PCB, Panasonic Electric Works, Part# JSM1A-12V-4, Catalog# 255-2223-ND	$1.30	$7.80
6	1	IC MUX/DEMUX ANALOG HS 24-SOIC, Texas Instruments, Part# CD74HC4067M, Catalog# 296-9225-5-ND	$0.72	$4.32
		Total		$522.01

Table 5. Prototype Sequencer Expense Table

III. SEQUENCER MECHANICAL PROPERTIES

A. DESIGN_NET MIPS MECHANICAL INTERFACE

To respect Design Net proprietary rights, the author will not detail the specifics of the Design Net MIPS mechanical interface. The company openly published minimal documentation describing the certain specifications and requirements for the company's sequencer. These requirements and specifications have been used throughout the engineering process to develop the mechanical, electrical, and functional components of the prototype sequencer. On that note, the functional requirements document for the NPSCuL-Lite prototype sequencer is in the appendix for further detailed information.

B. NPSCUL-LITE MECHANICAL INTERFACE

1. Sequencer Attachment to the NPSCuL-Lite External Wall

Beginning with a small scale view and leading into a large scale view, this section will introduce the reader to the various phases of component integration of the project. The sequencer will be mounted on the NPSCuL-Lite's positive Y-axis external wall. The sequencer's front connector plate shall face toward the NPSCuL-Lite's positive Z-axis. The NPSCuL-Lite coordinate system is shown in Figure 6.

There is a ten-hole footprint on the NPSCuL-Lite external wall. This footprint will match the footprint of the sequencer and will act as fastening points for the sequencer to the external wall. Several issues occurred in the construction of the mass model and integration with the NPSCuL-Lite structure. Detailed explanations will be given later on in this chapter.

The following conceptual diagram illustrates how the sequencer will be mounted to the NPSCuL-Lite positive Y-axis wall.

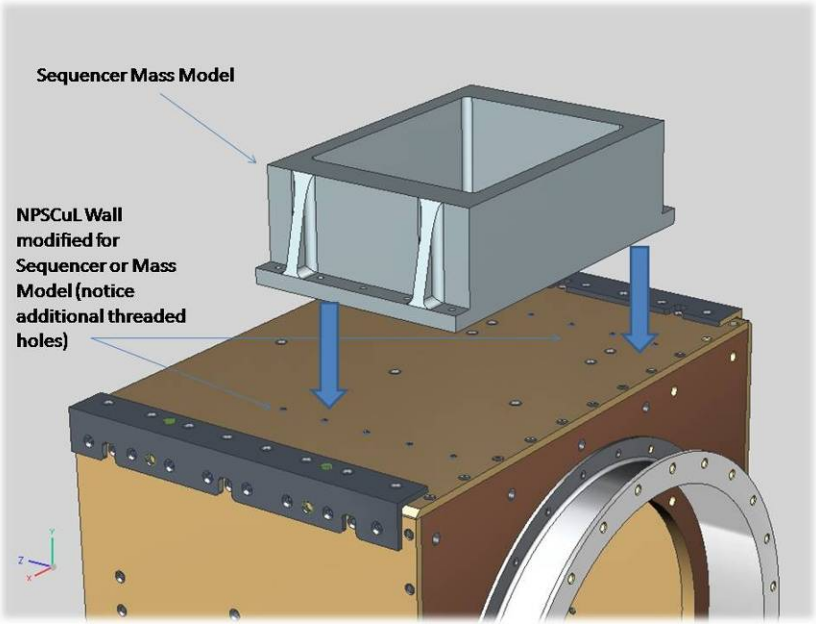


Figure 6. Sequencer Attachment to the NPSCuL-Lite Conceptual Diagram (From Crook)

The team designed several mass models during the development of the NPSCuL-Lite. After the physical creation of these mass models, the team proceeded to integrate these models in a fully integrated structure.

There are several purposes in creating mass models. One reason is for analysis and testing. Being able to examine a component on paper or electronically offers certain advantages. However, these forms of analysis offer distinct disadvantages. For example, an individual may find it difficult to grasp the overall dimension or the weight attributes. In addition, if one conducts tests on this structure, then subsequently does a post-test analysis, the examiner may not be able to mentally capture the extent of damage, deformation, or inherent weaknesses of the component without physically applying human senses to a physical object. Therefore, a mass model is utilized to reveal the above stated deficiencies.

Along the lines of testing, another example of the utility of mass models is structural testing. In order to perform structural testing, the inertial properties of the structure (the masses, dimensions, and the CGs) and the mechanical interfaces are all that are necessary for the designer to have. It would be imprudent not to commence testing

until final versions of all the constituent components are completed. It would be a waste of time considering that testing could be done earlier with rudimentary products.

Another reason that mass models are utilized deals with physical resources such as parts, components, or human labor. If the final design should fail during the final stages of project testing, this would mean that the engineers would have to spend more time and money purchasing, acquiring, and building the component again. Whereas, testing a mass model would only require minimal expenditures and effort. Moreover, this testing would provide certain definitive answers that may mitigate future resource costs.

The following photograph presents the fully integrated NPSCuL-Lite mass model structure.

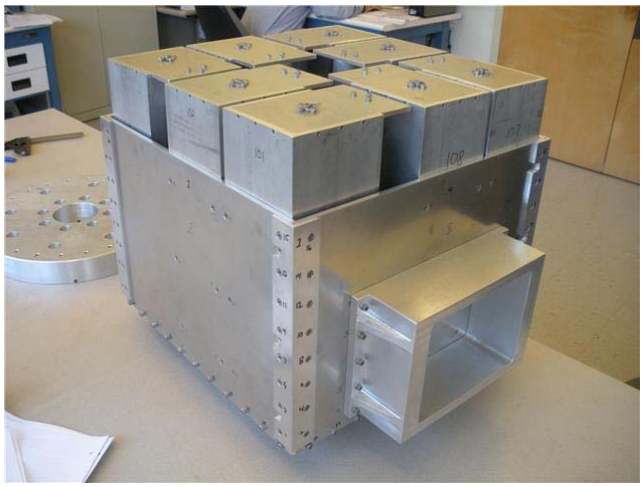


Figure 7. Fully Integrated NPSCuL-Lite Mass Model Structure

C. PROTOTYPE SEQUENCER MECHANICAL INTERFACE

1. Work Fall 2008

a. MIPS Conceptual Diagram

During fall 2008, Design Net released its "Deployment Subsystem Electronics (DSE) Requirements Specification" document that provided preliminary information on the future MIPS model. The document provides a conceptual diagram of the finished MIPS external chassis. The conceptual drawing is displayed below.

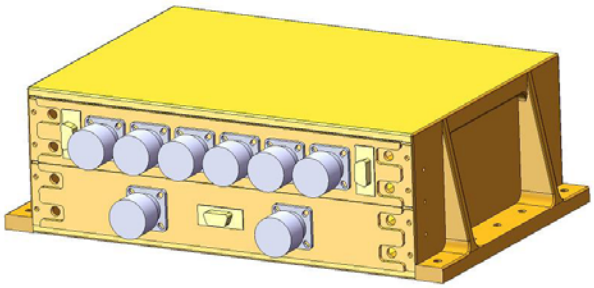


Figure 8. Design Net MIPS Conceptual Diagram (From Murphy)

The document does not provide much in regard to detailed information about the dimension attributes of the MIPS box. However, at this time the team at NPS had several discussions with Design Net personnel in regard to form, fit and function of the MIPS box. In those discussions, the team determined the structure's external dimensions. Using those specified dimensions, the author created a prototype CAD model box with similar dimensioning attributes.

b. I-DEAS Work for the Mass Model

Previously, the author started his initial CAD designs using the I-DEAS program. During this time, the author had enough preliminary information from Design Net to make a prototype model with similar dimensions. However, the placement of features and the relative sizing of features in respect to the working model's origin were unknown at this time. The MIPS box has side wall support features and clearance holes drilled into the flanges of the box. Since feature details were unknown at the time, the author extrapolated the sizing and placement of these features and composed them on the practice CAD model box.

Along with proper dimensioning, the author needed to create a model with similar inertial properties as the MIPS model. The CAD model needed to closely resemble these inertial properties in order to provide the closest fit for the NPSCuL-Lite project. Once again, some of this information was not revealed at this point of the project development. Therefore, the author had to extrapolate from known information at this time.

The mass of the model has a specific range based on Design Net's MIPS. The weight of the model ranges between 6 to 10 pounds (Salehuddin). The range is determined by several variables. The primary variables that would cause the most fluctuation in mass are the type of metal being used and the amount of electrical boards housed inside the MIPS box (Salehuddin). Considering this information, the author created more estimates. After the author conferred with an engineer at Design Net, Adi Salehuddin, it was determined that 10 pounds would be conservative final estimate of the box.

Using this information, the author manipulated I-DEAS to provide the proper weight amount while also maintaining the proper dimensioning elements. First, he used the appropriate function to assign aluminum 6061 as the structure's material. Then, the author vacated a hole originating from the Y-axis and milled down toward the –Y-axis until there was an empty void inside of the CAD model. The author conducted several iterations of this process, all throughout increasing and decreasing the shelf ledge widths on the Z and X-axes, until the resultant weight of the model fitted 10 pounds.

The following diagram manifests the work done on I-DEAS to create a Design Net-similar CAD model.

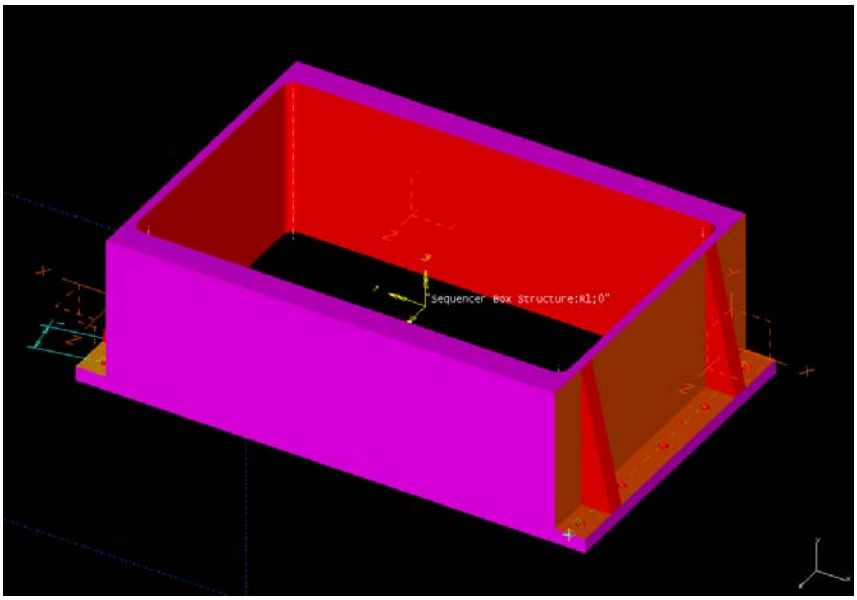


Figure 9. I-DEAS Prototype Sequencer CAD Model

2. Work Winter 2008-2009

a. Coordinate System of the MIPS Model and NX-6 Prototype Mass Model

At this point of the project, Design Net issued further pertinent MIPS related information and the author switched CAD model programs to develop further iterations of the prototype sequencer mass model. During this time period, Design Net disseminated the "Multiple Interface Payload Subsystem (MIPS) Envelope Drawing." This document elaborates on the feature size and placements of the final MIPS structure. Using this document, the author was able to correct the previous feature estimations and portray a model that was founded on actual parameters.

The first item of business was getting the appropriate features to be arranged correctly on the prototype model. The author concluded that the side wall supporting structure estimations were placed appropriately. Since these structures are not needed for the prototype sequencer, the placement of these elements is arbitrary. However, having the proper hole footprint is crucial for the NPSCuL-Lite design. The holes have to match the hole layout on the NPSCuL-Lite wall. Otherwise, the prototype sequencer will not fit; and, the entire NPSCuL-Lite project will be delayed until this issue is rectified.

Once the feature extrapolations were justified, the next step was to get the proper CG of the prototype. At this time, the author switched from I-DEAS to NX-6 CAD programming software. He composed another mass model using the same iterative approach used in I-DEAS to get the proper weight amount. After the creation of this model, the author spoke to Mr. Salehuddin to get the proper CG of the MIPS.

The Design Net engineers use a different X-Y-Z coordinate system than the author's model. The origin of the X-Y-Z axes of the MIPS structure is located in the center of the box exactly. Referencing the figure below, the Design Net employees have established the positive X-axis penetrating into the page toward the reader, the positive Y-Axis rises lengthwise up the page, and the positive Z-axis travels to the right of the page.

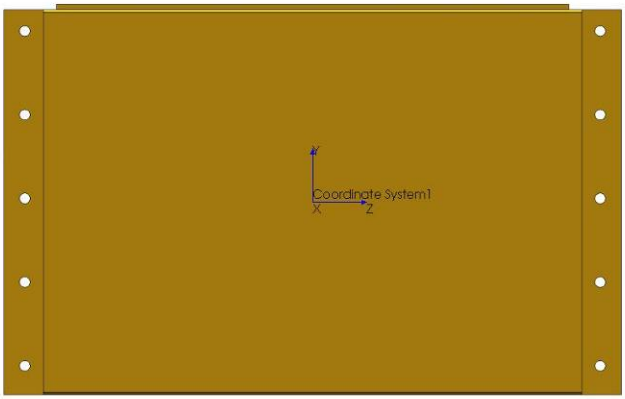


Figure 10. Design Net MIPS Box X-Y-Z Coordinate System (From Salehuddin)

MIPS Center of Gravity Coordinate System (inches)		
X	Y	Z
1.55	0.09	0

Table 6. MIPS CG Coordinate System (From Salehuddin)

In contrast, the prototype model has different positions for the X-Y-Z axes. The author used NX-6 software to make the next version of the prototype mass model. The origin of the X-Y-Z axes of the prototype structure is located in the center of the box exactly. The displayed coordinate system has the prototype positive X-axis matching the direction of the MIPS positive Z-axis, the prototype positive Y-axis matching the direction of the MIPS positive Y-axis, and the prototype positive Z-axis matching the MIPS positive X axis. This information will be helpful in understanding the discrepancies of the prototype characteristics explained further in this section.

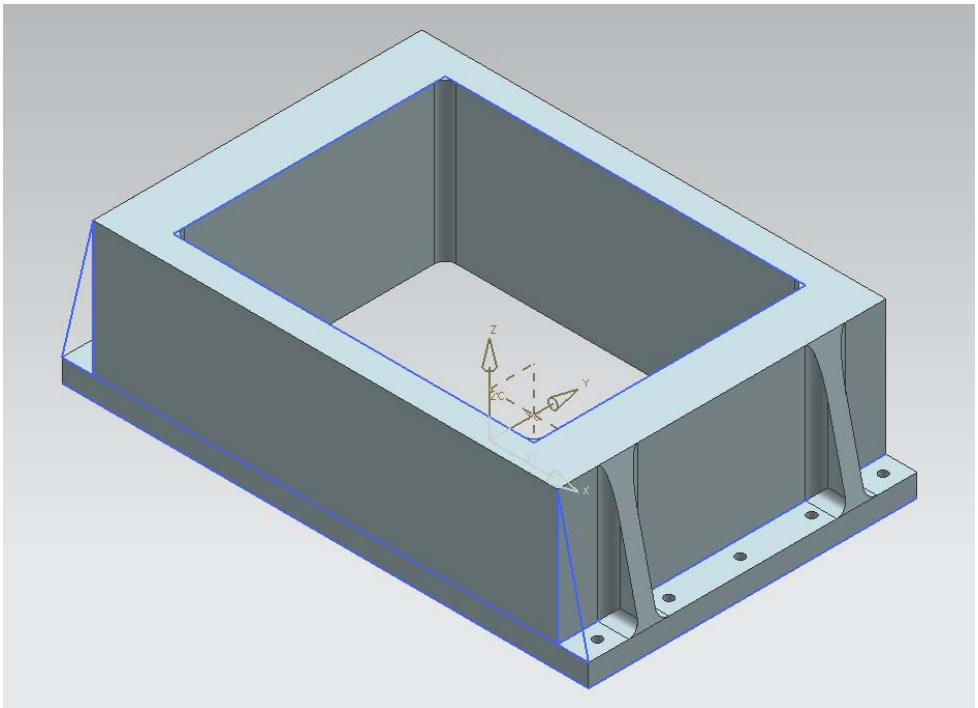


Figure 11. NX-6 Prototype Sequencer Mass Model Coordinate System

3. Work Spring 2009

a. Inertial Properties and Critical Issues of the Mass Model

Once the coordinate information was retrieved, the author performed inertial property analysis on ANSYS Incorporated engineering simulation software. The author gathered results concerning dimension attributes and inertial properties. The pertinent analysis conclusions are depicted below.

Material	Aluminum Alloy
Stiffness Behavior	Flexible
Nonlinear Material Effects	Yes
Bounding Box	
Length X	11.8 in
Length Y	7.36 in
Length Z	3.5 in
Properties	
Volume	103.01 in³
Mass	10.095 lbm
Centroid X	-5.2028e-017 in
Centroid Y	-1.0656e-004 in
Centroid Z	1.6729 in
Moment of Inertia Ip1	80.631 lbm·in²
Moment of Inertia Ip2	177.08 lbm·in²
Moment of Inertia Ip3	236.16 lbm·in²

Table 7. ANSYS Inc., Prototype Sequencer Structure Inertial Properties

Certain inertial elements do not match between the MIPS and the prototype. First, there is a discrepancy in the lengths between both models. Using the prototype's coordinate system as the reference frame, the X and Y coordinates displayed in the figure above match precisely between both models. However, the Z coordinate is off by 0.1 inch. Instead of having a Z dimension height of 3.6 inches, the mass model has a height of 3.5 inches that matches the MIPS model. The reason for this error is due to the author creating a dimensioning flaw when constructing the mass model on NX-6.

Second, the CG characteristics of the mass model and the MIPS are not exact. Once again using the prototype's coordinate system as the reference frame, the X and Y-axes are not exactly the same as the associated CG axes on the MIPS model. The MIPS model has its CG on the positive Y-axis displaced 0.09 inch from the origin. In contrast, the associated positive Y-axis on the prototype is displaced -1.0656×10^{-4} of an inch in from the origin. In addition, the MIPS model has its CG on the positive Z axis situated directly on the origin. Likewise, the Prototype's CG displacement on its associated positive X-axis is so small that it is virtually located on the origin as well. These are moot points considering each of the model CGs on their respective axes are so close to zero that one could essentially state that the CGs are located at the origin.

Furthermore, even fractions of an inch displacements from the origin will not disrupt the NPSCuL-Lite allowable CG displacement on the launch vehicle.

However, the largest CG displacement on both boxes may cause future issues. The CG displacement from the origin of the MIPS box in its positive X-axis is 1.55 inches. Whereas, the CG displacement on the associated Z-axis of the prototype box is 1.6729 inches.

This causes a couple of concerns. First, there is an approximate 0.12 inch difference between the CGs of both models. Considering this information, the prototype mass model is not fulfilling part of its mission by accurately reflecting the inertial properties of the MIPS box. However, this is almost a negligible concern. First, the Z-axis height difference is likely the main contributor to the CG offset. Some small variation may be attributed to the translation of the NX-6 file to ANSYS. Consequently, this mistranslation may have caused an increased simulated weight for the mass model. Second, the mass model's inertial properties are conservative. ANSYS simulates a 10.095 pound weight for the prototype mass model. The actual machined mass model weighs 9.9 pounds. Although the actual weight is lighter than expected, the weight still remains on the heavy extreme considering the inertial properties of the expected future product that the team will receive.

This issue is not necessarily a major concern. In fact, this issue may even prove to be beneficial for the team. It is a good systems engineering practice for one to make conservative assumptions during the preliminary designs of a project. In this situation, a conservative assumption is that Design Net's MIPS integrated structure will be expected to weigh more than the actual weight they will deliver. Therefore, when the final product is acquired, the team will have already taken the necessary steps to make the NPSCuL-Lite structure robust enough to handle a heavier sequencer. Therefore, the team will have a larger safety buffer in comparison to a situation where the team does not expect a heavier model. As a result, the measured weight of the prototype is not a major concern because the final MIPS that the team will procure will most likely be less massive. Therefore, the sequencer will pose fewer CG restrictions than the prototype mass model.

The other concern continues to deal with the prototype CG displacement in the positive Z direction in respect to the prototype coordinate system. ULA has given the team a certain inertial property envelope that the NPSCuL-Lite is required to stay within. The NPSCuL-Lite will breach the CG envelope on its respective Y-axis using the sequencer mass model.

This issue is a major concern in regard to project development. It is a major concern because there may be detrimental effects on the NPSCuL-Lite and the launch vehicle if this envelope is breached. Further investigation of this matter should be conducted by future team members.

The following chart presents the NPSCuL-Lite mass properties. The allowable NPSCuL-Lite CG displacement on the Y-axis is 0.5 inch. One can see that the heavy prototype mass model breaches that limit and pushes the axis displacement to 0.76 inch.

NPSCuL Lite Mass Properties						
				Center of Gravity		
Component	Volume (cubic inches)	Weight (lbs)	Weight (kg)	x	y	z
Adapter	33.42	3.38	1.53	0.00	0.00	1.02
Base Plate	104.86	10.59	4.80	0.00	0.00	2.35
Sidewall 1	59.21	5.98	2.71	9.12	-0.11	8.60
Sidewall 2	59.21	5.98	2.71	0.11	-9.13	8.60
Sidewall 3	59.21	5.98	2.71	-9.12	0.11	8.60
Sidewall 4	59.21	5.98	2.71	-0.11	9.12	8.60
Bracket 1	6.59	0.67	0.30	9.01	9.01	8.60
Bracket 2	6.59	0.67	0.30	9.01	-9.01	8.60
Bracket 3	6.59	0.67	0.30	-9.01	-9.01	8.60
Bracket 4	6.59	0.67	0.30	-9.01	9.01	8.60
Sequencer	103.01	9.90	4.49	0.00	10.92	6.78
P-POD 1		4.95	2.25	6.14	6.44	12.90
P-POD 2		4.95	2.25	6.14	1.21	12.90
P-POD 3		4.95	2.25	6.44	-6.14	12.90
P-POD 4		4.95	2.25	1.12	-6.14	12.90
P-POD 5		4.95	2.25	-6.14	-6.44	12.90
P-POD 6		4.95	2.25	-6.14	-1.21	12.90
P-POD 7		4.95	2.25	-6.44	6.14	12.90
P-POD 8		4.95	2.25	-1.12	6.14	12.90
3U CubeSat 1		6.60	3.00	6.25	6.44	10.99
3U CubeSat 2		6.60	3.00	6.25	1.21	10.99
3U CubeSat 3		6.60	3.00	6.44	-6.25	10.99
3U CubeSat 4		6.60	3.00	1.21	-6.25	10.99
3U CubeSat 5		6.60	3.00	-6.25	-6.44	10.99
3U CubeSat 6		6.60	3.00	-6.25	-1.21	10.99
3U CubeSat 7		6.60	3.00	-6.44	6.25	10.99
3U CubeSat 8		6.60	3.00	-1.21	6.25	10.99
Total		142.85	64.80	0.00	0.76	9.91

Table 8. NPSCuL-Lite CG Properties Displacement Chart (From Crook)

b. Mass Model Draft Views

Below are top, front, side, and isometric cutouts of the drafts of the prototype sequencer mass model. These cutouts show the reader different perspectives of the prototype mass model along with the associated dimensions of the device. The top view illuminates the hole pattern, the center cut-out, and general dimensioning referenced to the each of the centerlines.

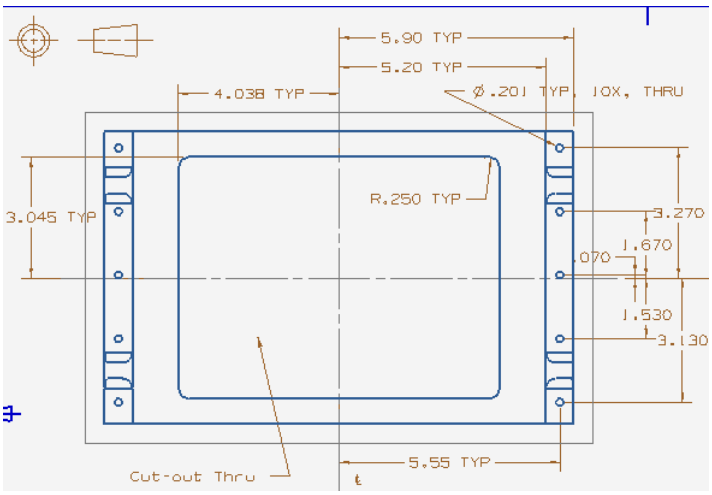


Figure 12. Top View of the Prototype Mass Model Draft

The front view of the prototype draft gives the viewer a physical understanding of the dimensions in this perspective. Furthermore, it provides the description of the angle dimension of the side support structures.

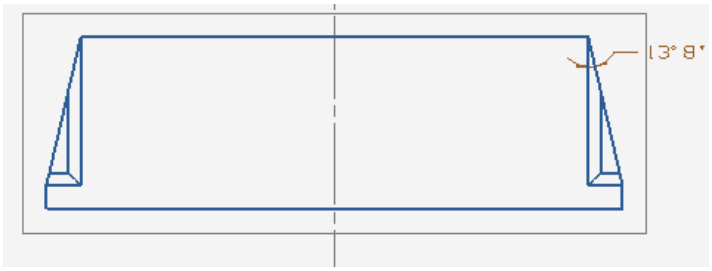


Figure 13. Front View of the Prototype Mass Model Draft

The side and isometric views of the prototype draft gives the viewer a physical understanding of the dimensions in these perspectives. The draft exhibits the prototype's height, length, location of the side support features, and the length of the flanges in respect to the illustrated centerlines.

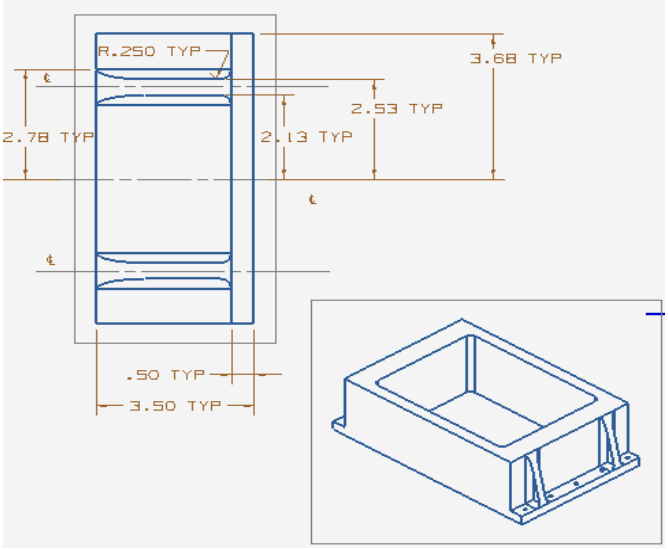


Figure 14. Side and Isometric Draft Views of the Prototype Mass Model

c. Mass Model Features

Once the drafts are refined into professional products, the designer is now ready to present the blueprints to the machinist for physical construction of the prototype. The prototype mass model is sculpted out of aluminum 6061 material. This material was not manufactured from metal made in the United States. Rather, it was made from foreign material in order to reduce expenses (Worth). Furthermore, it does not have any space qualified ratings. Therefore, the prototype mass model will not be used for anything more than analysis and testing.

Along with aluminum 6061, the author purchased 25 passivated A286 super alloy socket head cap size 10-32 screws to fasten the mass model prototype to the NPSCuL-Lite external wall. Unlike aluminum 6061, these fasteners are of a higher quality and have space qualification certifications (http://www.mcmaster.com/#socket-cap-screws/=27dme4).

4. Developing the Final Product

a. Final Prototype NX-6 CAD Model Structure

After the prototype mass model was constructed, the author began making preliminary designs of the final sequencer prototype. The final sequencer prototype will

have certain modifications with respect to the MIPS structure in order to support the mission of the NPSCuL-Lite project. The final sequencer prototype will be constructed in a way that will model the MIPS structure as closely as practicable, it will be constructed with a simplistic design to facilitate user operation and integration, remove internal and external flaws to allow for proper operation, and finally allow ease of removal and attachment of the electrical testing board. Although this design has certain replicated attributes from the mass model and the MIPS box, it differs from both models in several different ways.

The final model has certain similarities in regard to the prototype mass model and MIPS structure. It has the same external width, and length dimensions although the height varies by 0.12 inch. It has a hole pattern that is corrected to 5.5 inches from the vertical centerline dimension. Finally, the side support structures are identical among all models.

However, there are several inherent differences between the MIPS and final prototype models. First, the front view of the final prototype has been altered to fit testing needs. Referencing the MIPS conceptual diagram, the MIPS structure has 3 D-subminiature (D-sub) connecting interfaces and 8 Glenair circular connectors embedded on the front face plate. These connections will provide launch vehicle communications interfaces, a programming interface and power.

In contrast, on the final prototype model, the author modeled 8 D-sub connectors that will simulate launch vehicle communication interfaces, 1 Glenair connector for a power interface, and 1 D-sub connector for reprogramming. The type of Glenair connector is still unknown at this point. Therefore, this attribute will be addressed by future team members.

The following photograph illustrates the final prototype front face plates and the connector cutouts. From left to right, the diagram displays 8 simulated launch vehicle D-sub connectors, 1 Glenair Connector for power, and 1 D-sub connector for reprogramming purposes.

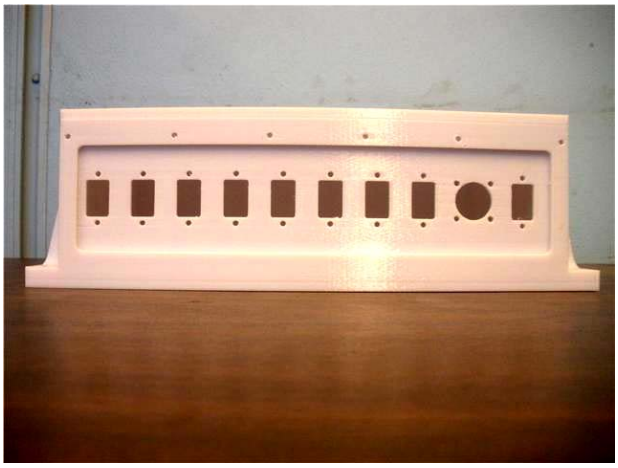


Figure 15. 3D Model Final Prototype Front Face Plate Connector Cutouts

Referencing the following diagrams, the author will depict the comparisons and modifications of dimensions and features between both models. The MIPS front face plate exhibited below is simply the drafting version. Therefore, the only information it offers is the length and height. The reader may examine the MIPS conceptual diagram to aid in his understanding in the following description.

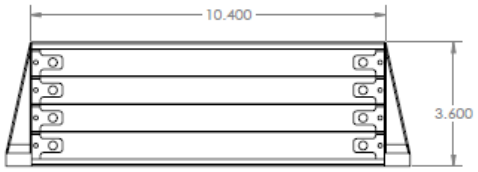


Figure 16. MIPS Front Face Plate (From DNet # 11050: Multiple Interface Payload Subsystem Envelope Drawing)

b. Modifications Made to the Front Face Plate

As mentioned previously, the final prototype has some modifications. The holes on the protruding ledge of the front face plate are debris evacuation holes. Drilling holes is a common hazard in creating metallic housings (Rigmaiden). Every time a hole is drilled, metal shavings are created, hidden, and often dispersed throughout the entire structure (Rigmaiden). This can pose certain electrical hazards such as shorts or equipment malfunction (Rigmaiden). Therefore, it is necessary to have these external holes to provide an opening for metal shavings and other debris to escape.

Other modifications on the final model are the recessed face and the connector cutouts on the front face plate. The final prototype has a $^{1}/_{8}$ inch recessed face. This face contains the several different connector cutouts that will attach to the internal electrical testing board. The holes that are symmetrically placed to each respective cutout exist for connector fastening purposes.

The following illustration contains the attributes of the front face plate of the prototype sequencer. It contains fillet, hole, cutout, and general feature dimensions.

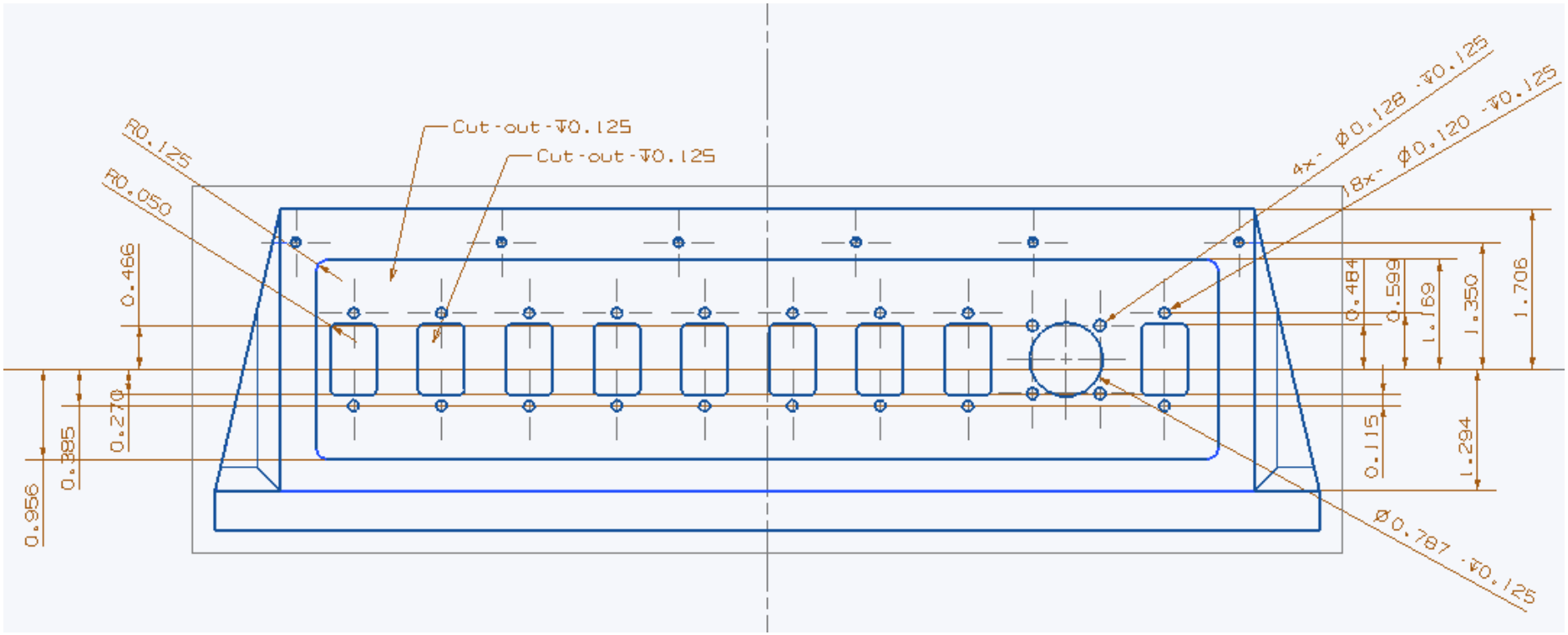


Figure 17. Final Prototype Front Face Plate Part 1

c. External Draft Views of the Final Prototype

Part 1 of the schematic focuses primarily on the fillets, holes, and connector cutouts. Part 2 focuses on the dimension nuances of the internal and external overall structure. The following draft represents Part 2 of the front face plate.

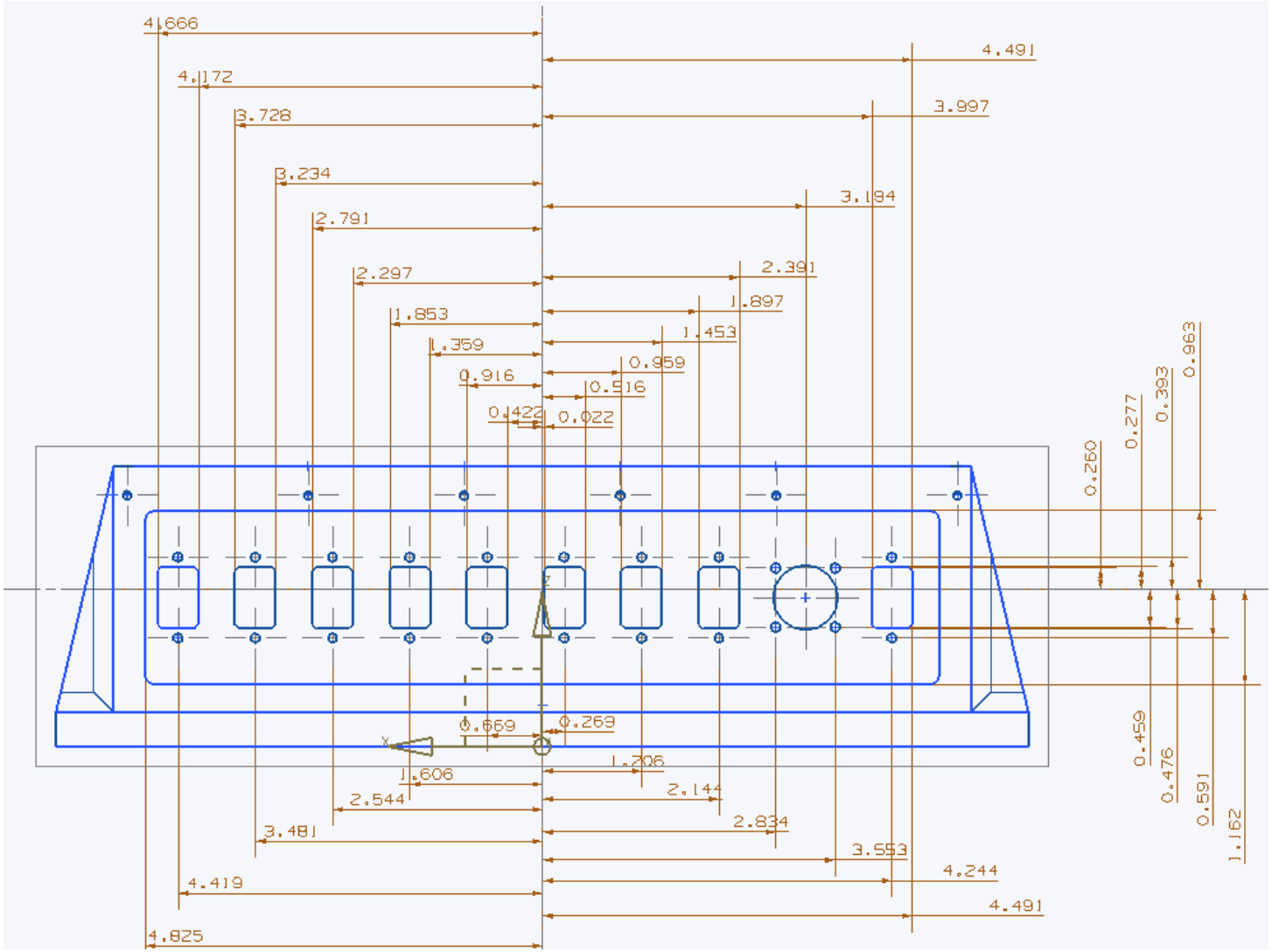


Figure 18. Final Prototype Front Face Plate Part 2

The next section to be discussed is the side perspective of both models. In this perspective, both models have identical characteristics. The side perspective of the final prototype displays evacuation hole properties, flange sizes, feature dimensions referenced from the centerlines, and general external dimensions.

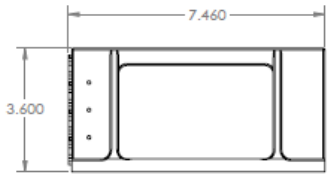


Figure 19. MIPS Side View Draft Cutout (From DNet # 11050: Multiple Interface Payload Subsystem Envelope Drawing)

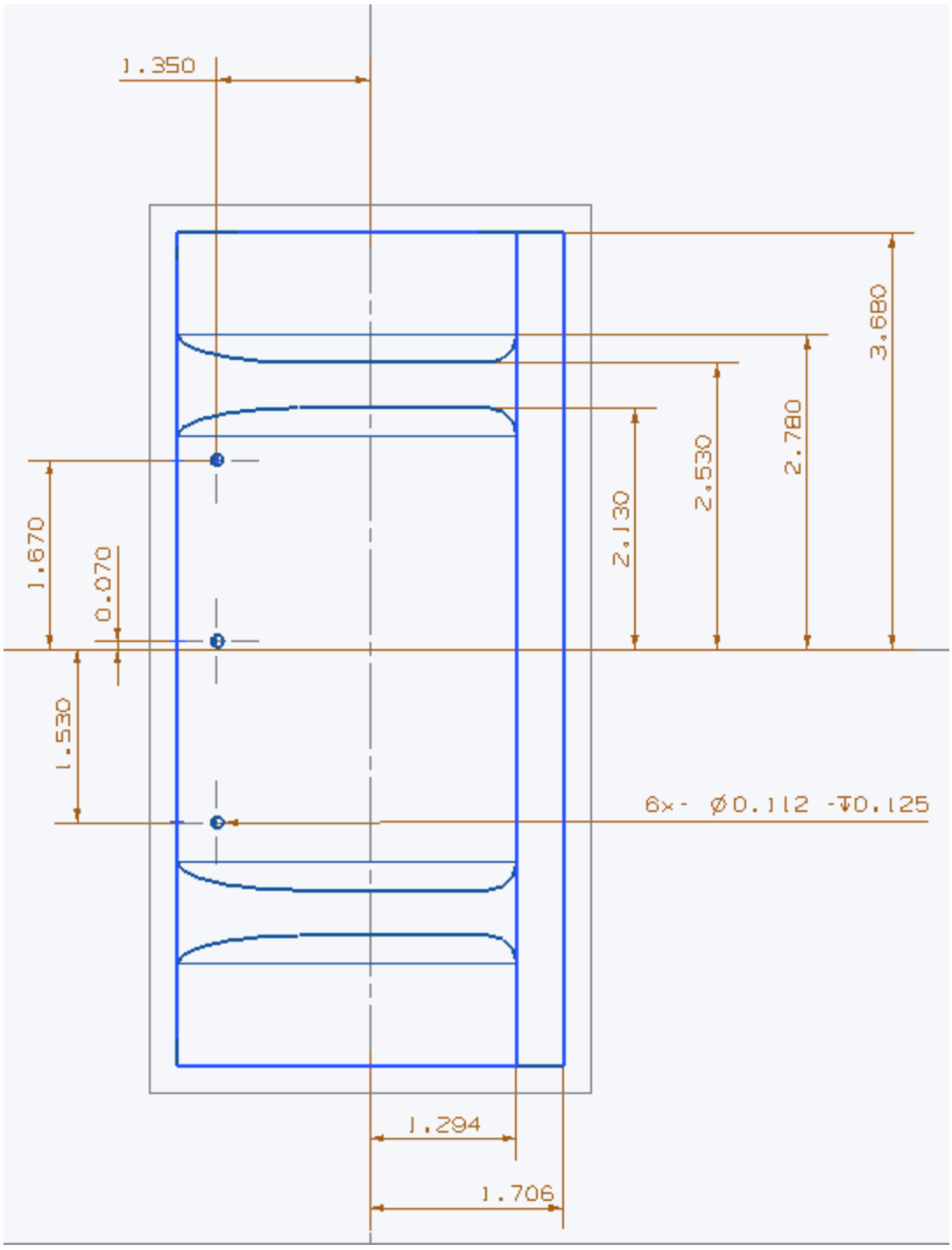


Figure 20. Final Prototype Side View Draft Cutout

The top view is the final aspect that will be examined. The final prototype structure and the MIPS box have identical top view dimensions and attributes. Therefore, only the MIPS box with draft cutout will be displayed. The MIPS container flange hole

pattern and properties are displayed below. This hole pattern is symmetrical about the vertical centerline of the MIPS box. These features are illustrated in the following MIPS structure draft cutout.

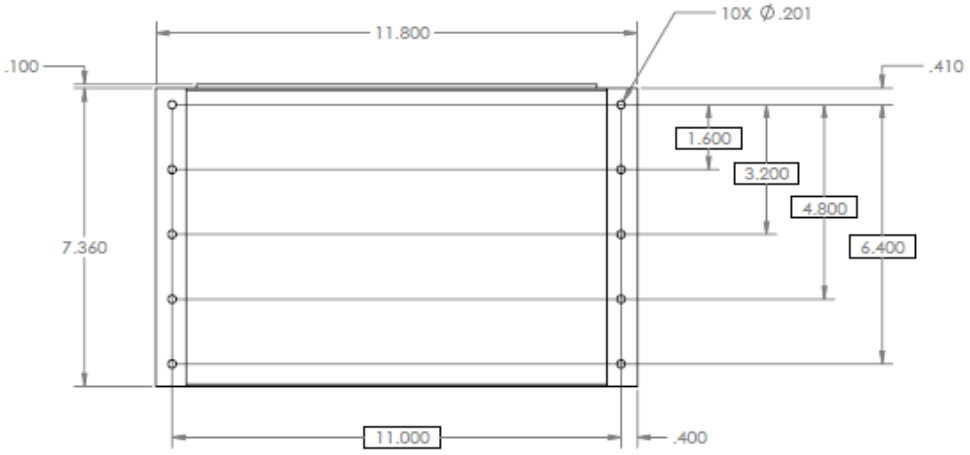


Figure 21. Top View of the MIPS Structure Draft Cutout (From DNet # 11050: Multiple Interface Payload Subsystem Envelope Drawing)

d. Internal Draft Views of the Final Prototype

The associated view of the final prototype chassis has some similarities and differences with the MIPS chassis. Once again, the flange hole properties and footprint matches identically to the MIPS model. In addition, the general external length and width dimensions are congruent with the MIPS model.

However, there are several modified features implemented in the final prototype. First, there are two internal cutouts to support the electrical board. The following illustration displays a small cutout, large cutout, and additional key chassis features. The small cutout exists to allow sufficient space for the wiring harness to connect the mounted face plate connectors to the printed circuit board (PCB). The large cutout exists to act as a supporting shelf for the PCB during mechanical and electrical integration and testing. Other chassis features will be discussed further in this chapter.

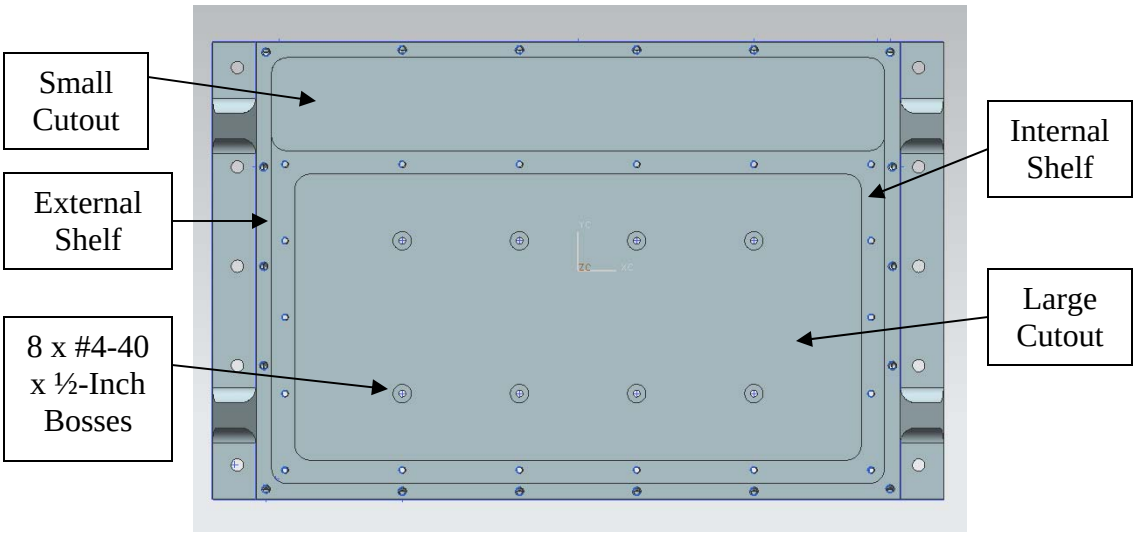


Figure 22. Conceptual Diagram of Key Internal Chassis Features

Other modifications that exist on this board are the addition of a variety of holes. Starting from the inside center of the large cutout and progressing outward, there are eight #4-40 threaded bosses (or standoffs), ½-inch in length, used to fasten the PCB itself, and may be used to attach larger components.

Moving even further outward from the erected cylinders, there lies a shelf with eighteen #4-40 tapped screw holes. Similar to the function of the cylindrical shells, these holes offer a place to fasten the PCB to the final prototype chassis. The PCB will rest on this internal shelf and completely cover the large cutout. The small cutout will remain uncovered for wire harnessing purposes. Future iterations of the PCB will have eighteen #4-40 tapped screw holes fastened to align with the screw holes on the internal ledge. Furthermore, the board will also be fastened to the eight #4-40 standoffs of ½-inch length from the base of the box. This additional fastening will increase board stability during future vibration testing and increase heat transfer from the board-mounted electrical components to the sequencer chassis.

The following illustration provides a conceptual understanding of how the PCB will attach to the internal shelf. The prototype PCB is still in its nascent stages of development. Therefore, the exact knowledge of the type of components being used, the placement of these components, and feature modifications to the sequencer chassis are not known at this time. Considering the project's limited development, several elements

of the PCB and/or the prototype chassis can change dramatically. Thus, the author created only a rudimentary board with the proper dimensions to fit on the internal shelf.

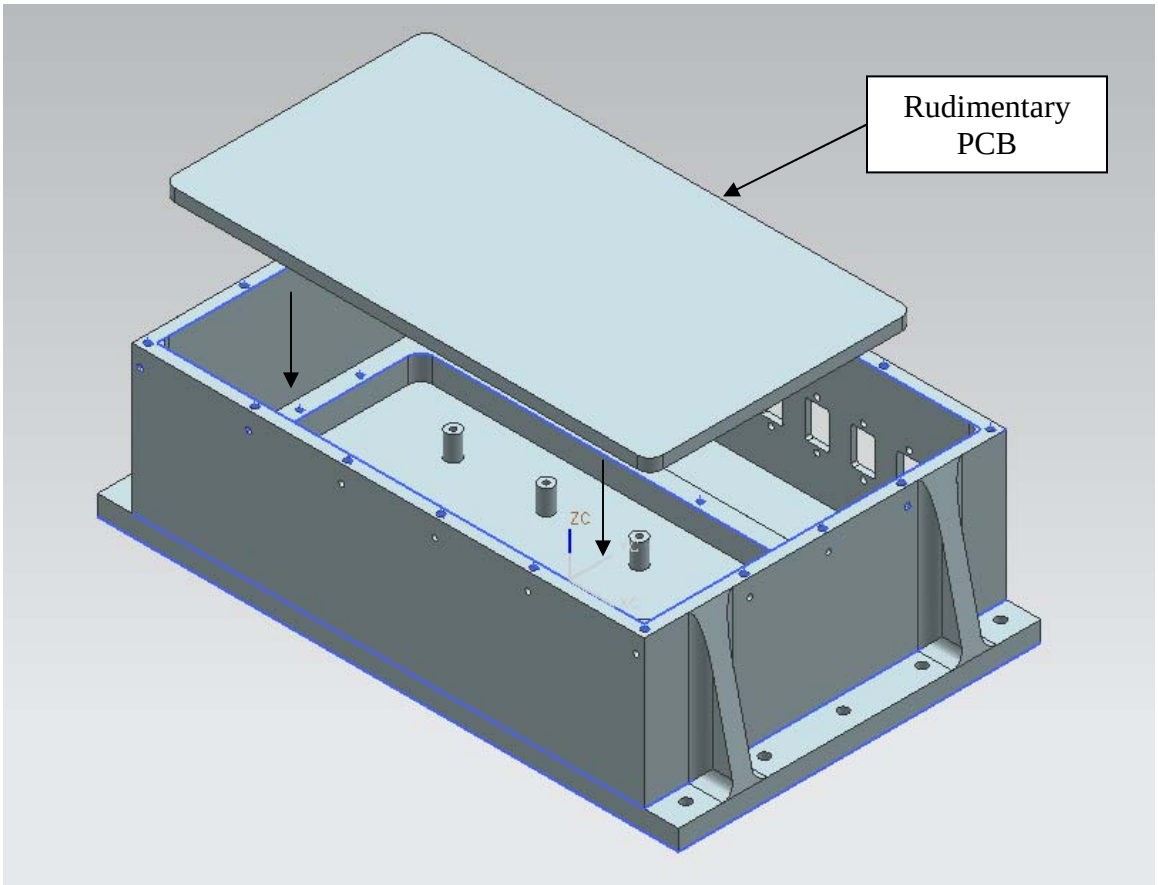


Figure 23. Conceptual Diagram of the PCB Attachment to the Internal Shelf

Finally, the structure contains an external ceiling shelf that contains the two cutouts within. This external shelf is mounted at the top of the box. It contains eighteen #6-32 tapped screw holes to match the hole size and footprint of the final prototype lid.

More errors were created on the final prototype box. Every tapped hole in the box that exists to fasten another structure in place is too small. The author attempted to fit the appropriate screws in the holes and concluded that the screws are significantly larger than their respective hole diameters on the structure. The understanding behind this issue has not been revealed at this point. Possibly, there may be an interfacing issue between NX-6 and the 3D printing machine. Or, the accuracy of the 3D printer may not

be high enough to create the proper hole diameters. Or, it can be simply an error created by the modeler himself. All in all, this issue should be investigated by future members of this team.

The following top view cutout of the final prototype elaborates on the above mentioned detail including further elaboration on feature properties and dimension attributes.

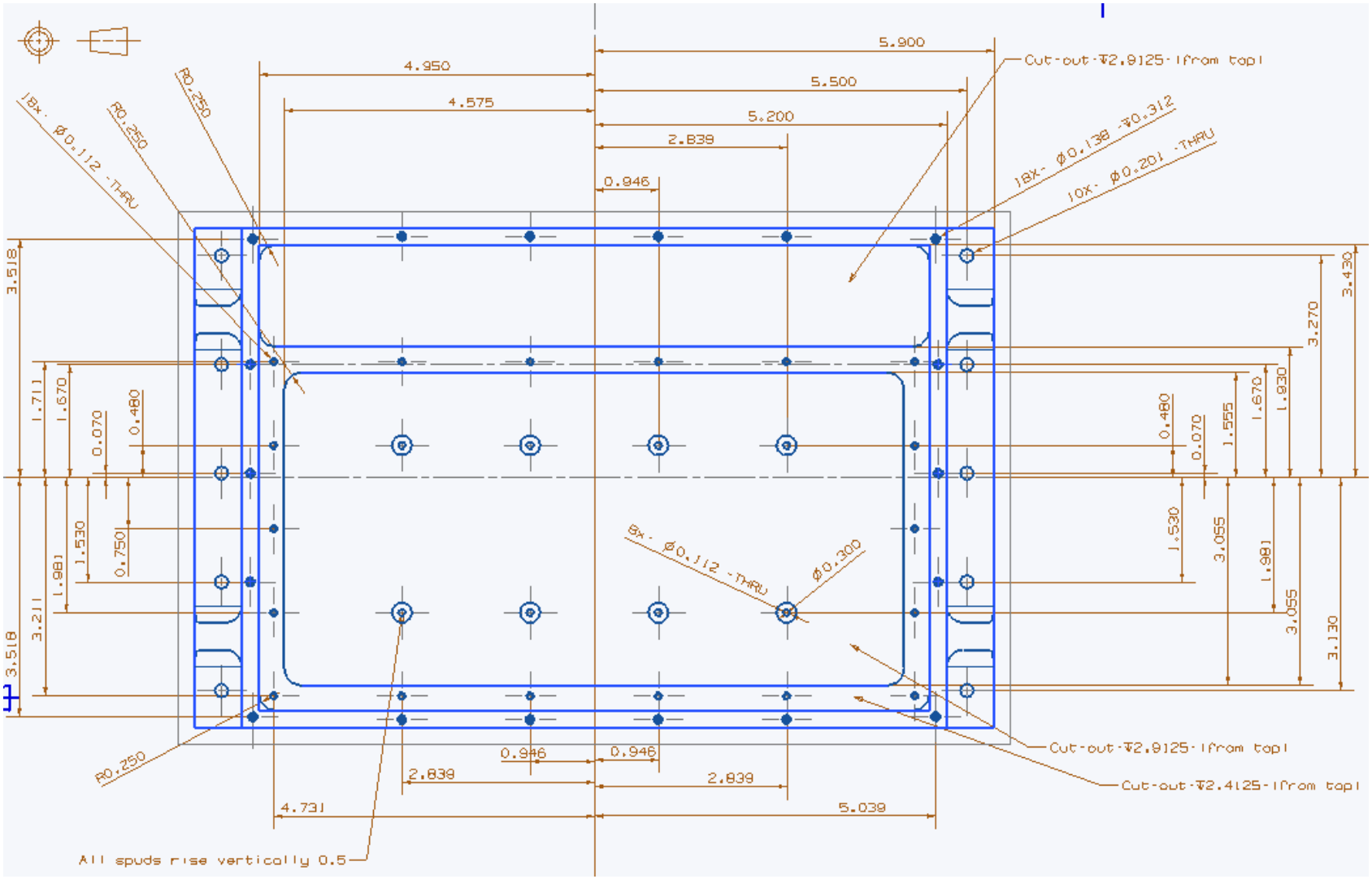


Figure 24. Top View of the Final Prototype Draft Cutout

e. Prototype NX-6 CAD Model Lid

As mentioned before, the final prototype chassis has a lid that rests on an external shelf. This lid exists to protect the internal PCB and electrical components from the outside environment. Likewise, it exists to protect the safety of external users from live electrical equipment. The lid has the same issue as the main chassis in regard to improper hole sizing. This issue will be examined by future students.

The following three draft profiles express the necessary feature properties and dimensions of the final prototype lid.

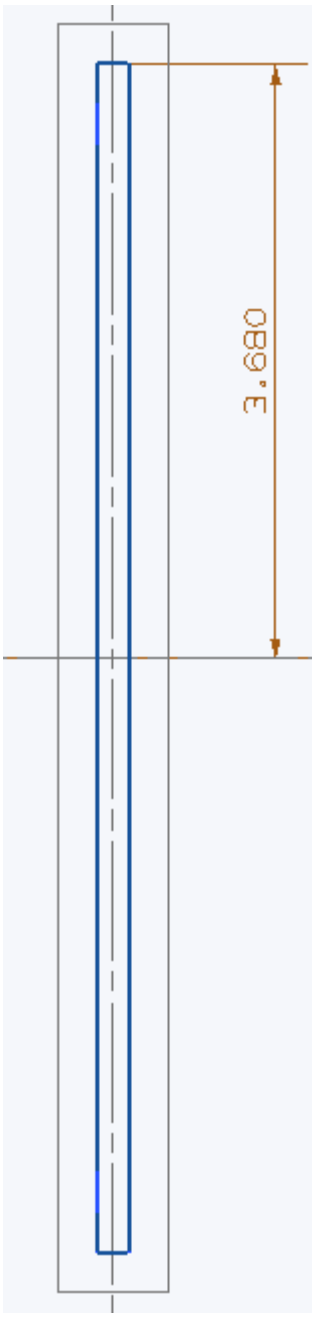


Figure 25. Final Prototype Lid Y-Axis Draft Cutout

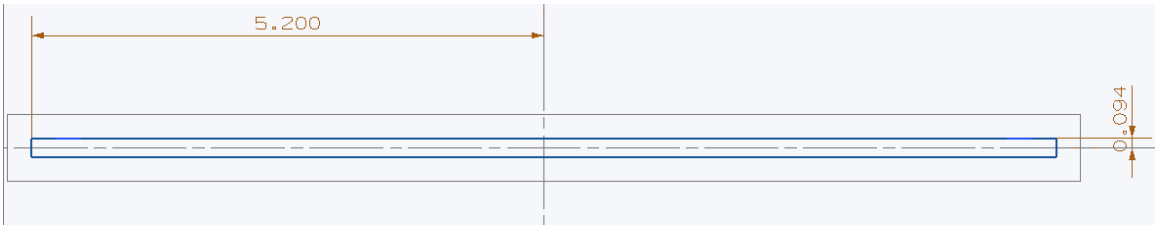


Figure 26. Final Prototype Lid X-Axis Draft Cutout

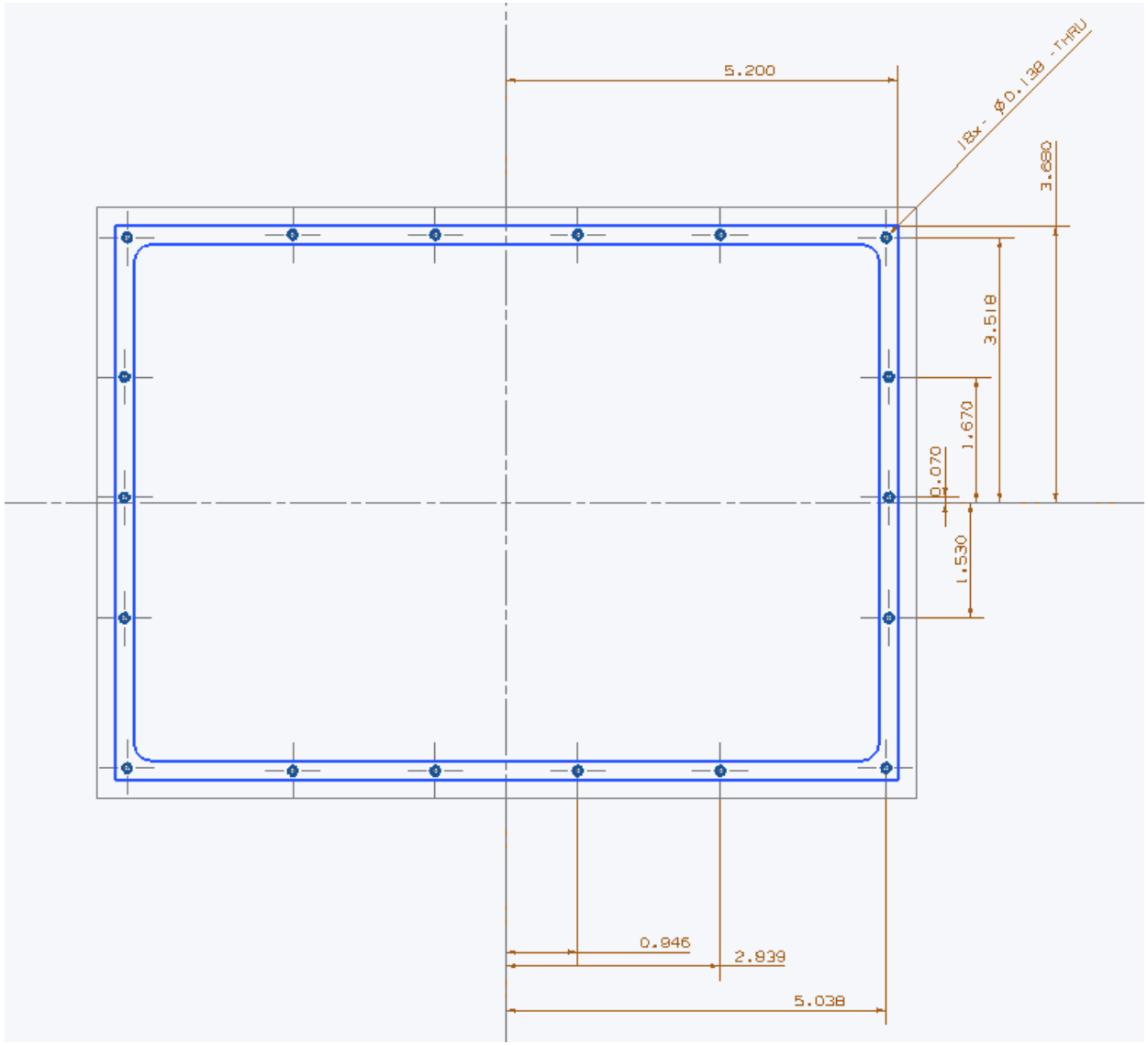


Figure 27. Final Prototype Lid Top View Draft Cutout

IV. SEQUENCER ELECTRICAL PROPERTIES

A. NPSCUL-LITE ELECTRICAL INTERFACE

1. Design Net Multiple Interface Payload System (MIPS) Electrical Interface

Because of Design Net proprietary protection, the author will not detail the specifics of the Design Net MIPS electrical interface. The company published minimal documentation describing the certain specifications and requirements for the company's sequencer. These requirements and specifications have been used throughout the engineering process to develop the mechanical, electrical, and functional components of the prototype sequencer. On that note, the functional requirements document for the NPSCuL-Lite prototype sequencer is in the appendix titled, "NPSCuL-Lite Prototype Sequencer Functional Requirements Document," for further detailed information.

2. P-POD NEA

An electrical interface is required to open the P-PODs. This interface is called a non explosive actuator (NEA). Initially, the launch vehicle provides 28V to the sequencer. The sequencer becomes energized and distributes the received power to the necessary components of the circuit. Then, the launch vehicle sends a "fire" signal through another circuit to initiate the sequencer program execution. When that "fire" signal is executed, 28V 6A power is allowed to actuate the individual NEAs.

The following photograph shows two NEAs. They are 1.70 inches in diameter and 1.56 inches in height. The NEA on the right displays the hole that accommodates a #1/4-28 bolt.

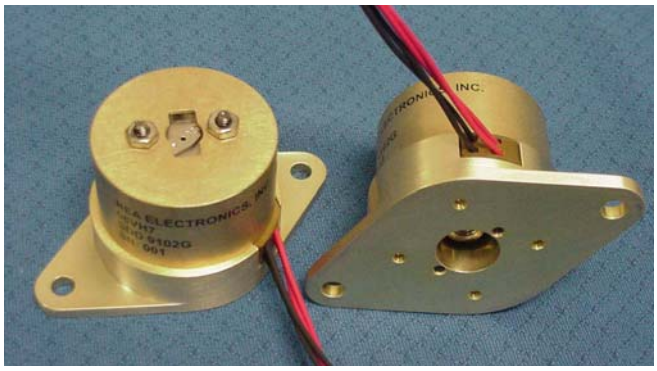


Figure 28. NEA (From Model 9102G: Nonexplosive Release Mechanism (.250-28 Thread))

The NEAs are non-explosive for a specific reason. The payload has to be kept in a safe condition. An explosive actuator would create unnecessary and undesired shock to the P-PODs and the internally housed CubeSats (Schaffner).

A deployment sensor is installed on the P-POD doors (Lan). This mechanism provides an indication to the sequencer and subsequently the launch vehicle when the doors are opened (Lan). When the door opens, the switch changes states, and a "door open" reading is delivered to the sequencer and subsequently the launch vehicle. The Honeywell 3M1 switch and the Saia-Burgess snap-action switch both have been used operationally for P-PODs (Lan).

Each NEA has a primary and redundant circuit with primary and redundant heating elements respectively. A redundant signal is implemented to ensure proper actuation of the circuit. However, only one circuit is needed to allow the opening mechanism of the P-POD to function. Each circuit has a heating element that actuates when it receives a signal. Once the heating element actuates, the P-POD doors open, the normally closed switch opens, and telemetry is sent back to the launch vehicle.

The following conceptual circuit depicts the inner workings of the NEA release mechanism.

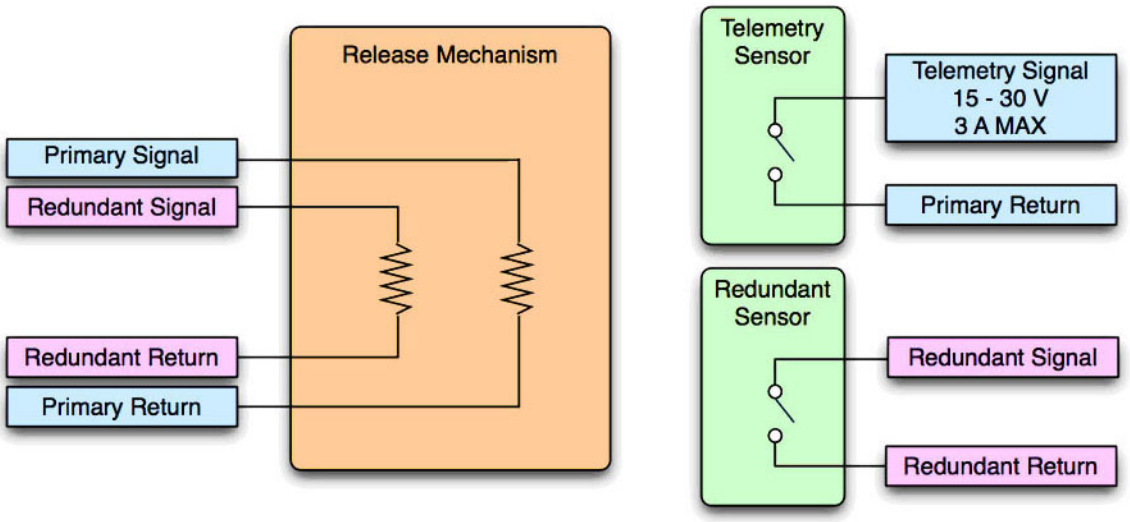


Figure 29. NEA Conceptual Circuit (From Lan)

The NEA has certain electrical specifications stated below. The NEAs are rated to fire when they receive a 4A signal for each circuit. Since there are two circuits, the total amount of current equals 8A. With this current rating, the opening mechanism would require only 12 to 15 msec (Coelho). However, the NEAs can fire with as little as 2A (Coelho). Using this current rating, the opening mechanism would require 100 to 120 msec (Coelho).

The following chart compares the features of two distinct P-POD opening mechanisms. Currently, the Starsys Qwknut 3k release mechanism is not an option for the scope of this project. Its specifications are provided only as a reference.

Release Mechanism Specifications				
Release Mechanism	Resistance Range (Ohms)	Signal		
		Current Range (A)	Voltage Range (V)	Actuation Time (ms)
Starsys Qwknut 3k	3.9 – 4.1	3.5 – 5.5	15-21	100
NEA 9102G	1.2 - 1.6	2.0 – 20	3.0 - 30	45

Figure 30. Feature Comparison of Release Mechanisms (From Lan)

B. PROTOTYPE SEQUENCER ELECTRICAL INTERFACE

1. Work Fall 2008

a. Microsoft Visio Conceptual Electrical Design

In Chapter II, the author details the process in which the project developed over time. In this section, the author will describe the electrical development process of the prototype sequencer in more detail. During fall 2008, the author was working with dual purposes simultaneously. The first purpose was to learn how to model a sequencer box through a CAD programming module. The second purpose was to develop an electrical interface starting with rudimentary flow diagrams that outlined the basic sequencing processes. The end result of the second purpose aims to devise a simplistic, systematic, and requirement-fulfilling approach that would result in the physical construction of an electrical PCB to manipulate the previously mentioned P-POD NEAs within their respective design parameters. In this section, the author will not elaborate on extensive electrical details for the sake of staying within the scope of this thesis. Rather, the author will attempt to provide a basic understanding of the electrical work development in fall 2008.

The author capitalized on several tools to complete this preliminary task. First, during independent study, the author gained the necessary insight on wiring, basic circuit knowledge, microcontroller programming, and an introduction to CAD programming to theorize a proper flow path. Second, several interactive discussions took place that gleaned possible internal circuit components that would fulfill the sequencer mission.

For example, the author discovered through those discussions that a 28 V power supply would be required to open a P-POD door. An external voltage regulator is required to step down the voltage to operate internal circuitry at appropriate levels. A properly configured push button circuit is required. A Stamp microcontroller with internal programming is needed. Finally, other internal electrical components such as relays, relay drivers, integrated circuits, transistors, and other basic components are required to accomplish the mission.

The following diagram illuminates the basic conceptual flow path of the prototype sequencer.

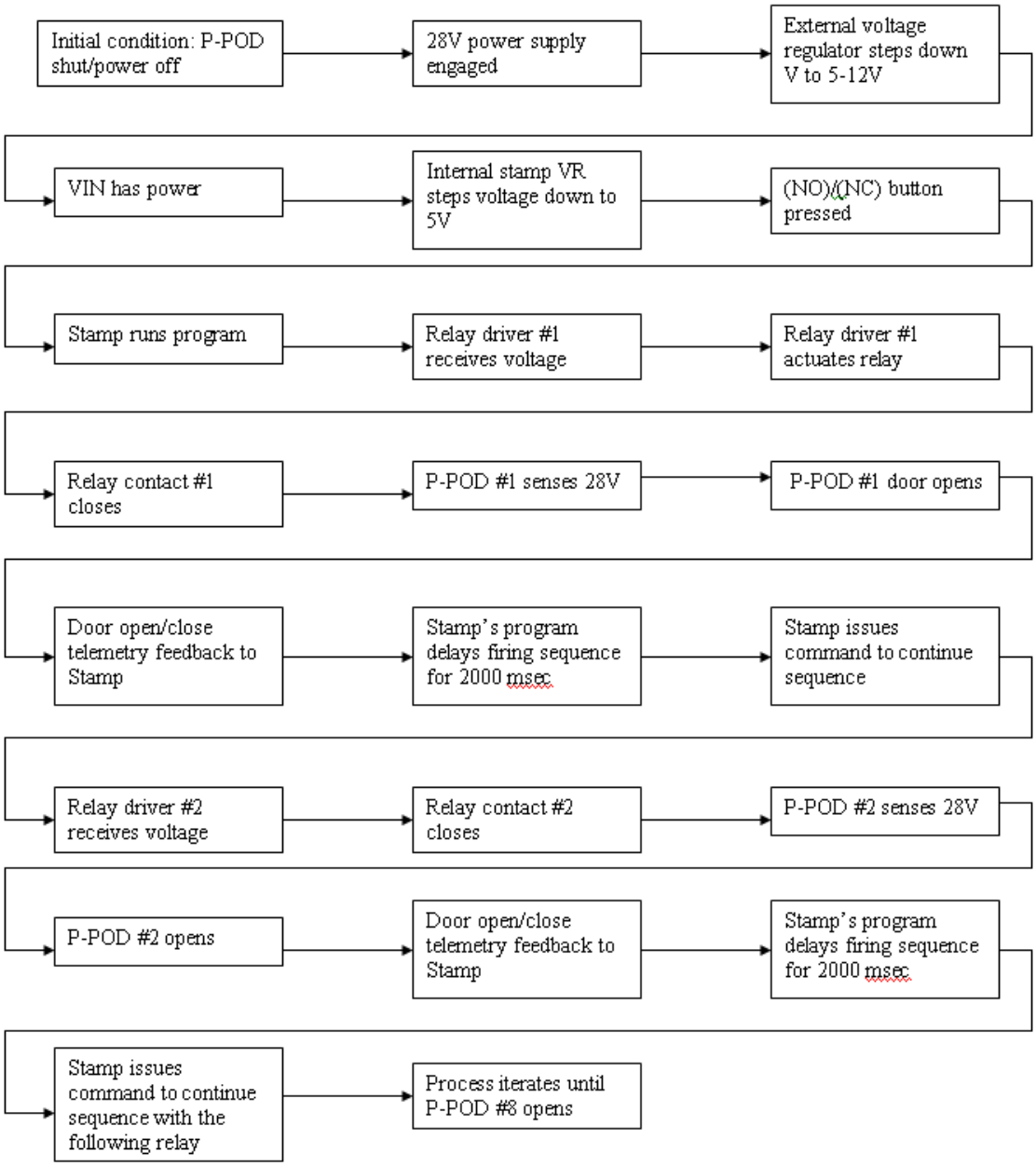


Figure 31. Prototype Sequencer Flow Path

Certain physical mechanisms occur during the evolution of the flow diagram. Initially, no electrical power is present in the sequencer and all P-POD NEA circuitries. Therefore, each P-POD door is initially shut. When the PCB receives 28V, the voltage is regulated by an external voltage regulator to 12V. The BS2 Stamp receives

this voltage and becomes energized. Its associated "VIN" pin-out receives this voltage and steps down this voltage to 5V by its internal voltage regulator. The 5V output is then delivered to pre-designated pin-outs for internal circuitry manipulation.

The internal circuitry is configured in a manner that will actuate the NEAs of the P-PODs. The "VDD" pin out provides the source voltage to push buttons and relay drivers directly. The microcontroller will operate the high load relays indirectly via the respective relay drivers. The microcontroller has to operate the relays indirectly because the amount of output current and voltage of the basic Stamp are insufficient to drive large loads. Once the relays are energized, an internal solenoid will close a relay contact, and a 28V 2A power will energize the NEA heating elements. The procedure iterates until all the P-POD door mechanisms are open.

2. Developing the Final Product

a. Primary Test Board (PTB)

After preliminary flow diagrams, schematics, and tests, the author and Mr. Justin Jordan began developing the PTB. The author provided Mr. Jordan with a functional requirements document. Mr. Jordan translated the requirements specified in the document into schematics, electrical components, and a properly configured PTB.

Considering the scope of this thesis, this chapter will not contain the full technical specifications and descriptions of each of the electrical components mounted on the PTB. Many electrical components that are mounted on the PTB will not be discussed. Although these components are necessary for proper board operation, the author feels that these components are adjunct to key drivers of the circuitry. Moreover, elaborating on the technical specifications of these components will not be within the scope of this thesis. However, some additional technical details can be found in the "NPSCuL-Lite Prototype Sequencer Functional Requirements Document," and the "NPSCuL-Lite Prototype Sequencer Electrical Board Unit Thermal Acceptance Test". On this note, full schematics are also found in the associated appendices. Finally, the reader may find all the source information of every component used in the creation of the PTB in the "List of References" section of this thesis.

The conceptual operation of the board is specified several times in this thesis. It is detailed in the flow chart in the section, "Work Fall 2008," the FRD in the appendix, and in the thermal-vacuum testing document. Therefore, the author will not include a duplicate flow chart in this chapter.

In the order of operation, this section will introduce the reader to the components, their respective placements on the PTB, and a general description of the primary components and circuitry. The author will provide cutouts of the schematics and the PTB during the component description to facilitate the reader's overall understanding of the circuitry as a whole.

The PTB can be summarized as having eight dissimilar circuits intended to accomplish the same mission. Eventually, a fully developed prototype sequencer will be able to manipulate the opening mechanisms of 8 P-PODs and provide telemetry feedback of each. However, the current level of development of the prototype sequencer is not at this level of sophistication. The mission of the current prototype sequencer is to actuate eight relays that will in turn actuate other associated circuitry to allow eight 28V 2A signals to reach their associated P-POD NEAs.

Each circuit contains different COTS electrical components. The reasoning behind having dissimilar components in each circuit is for testing purposes. In order, to create the highest quality test board, the operator must test each component to verify which component and/or circuit accomplishes the task in the most efficient and effective manner. Applying thermal/vacuum, pressure, acoustic and other space qualifying acceptance and qualification testing will determine which components offer the best results. The following chapter will discuss testing of the PTB in detail.

The following photograph shows a top-down overall view of the PTB and all the integrated circuitry.

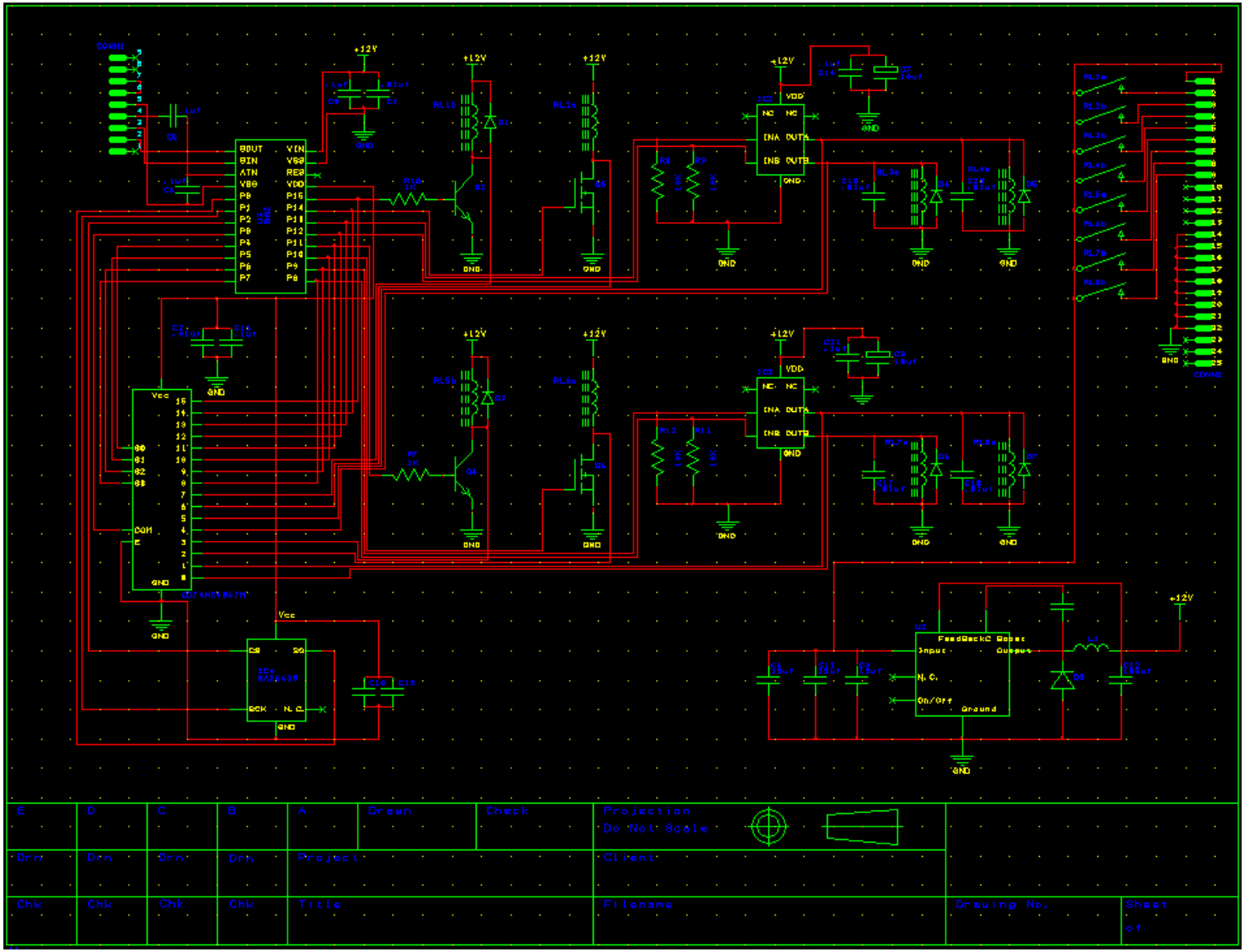


Figure 32. Complete PTB Electrical Schematic

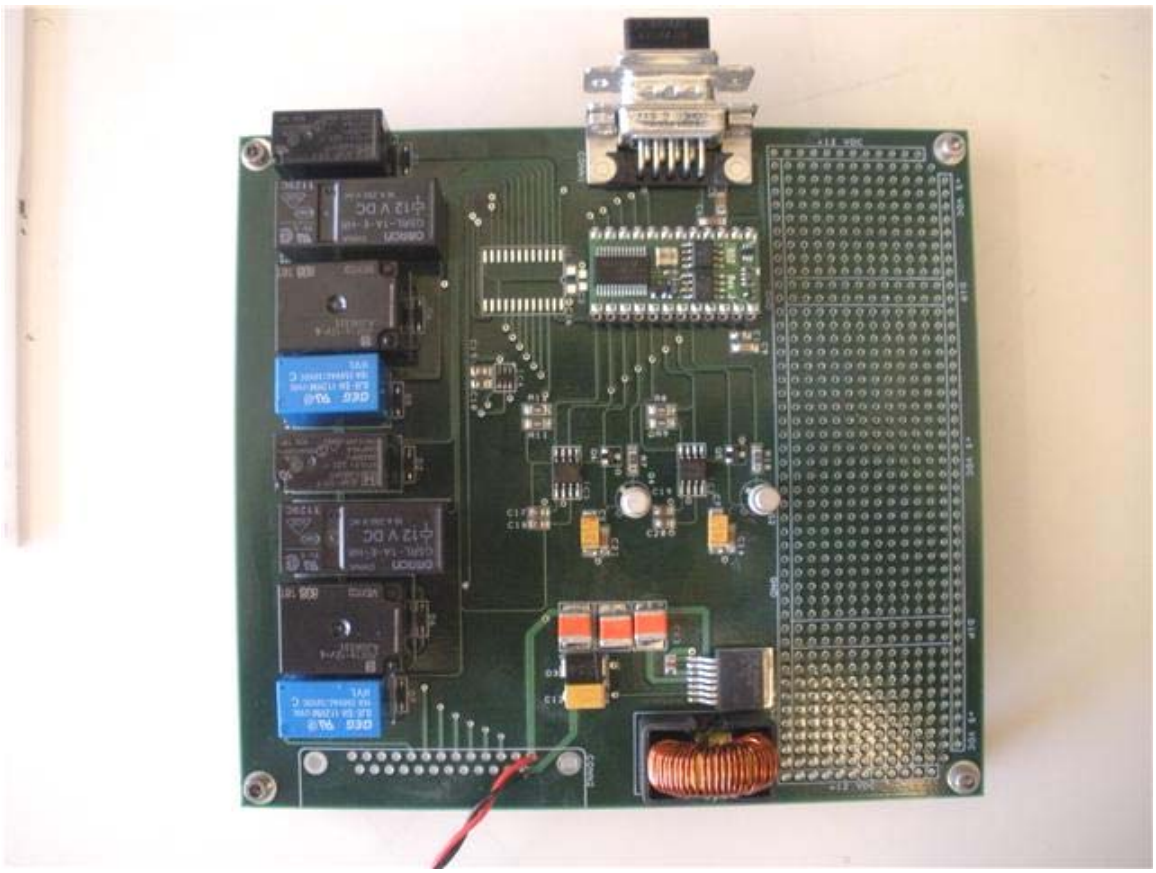


Figure 33. Fully Integrated PTB

b. Power Supply

The PTB requires power for any of the functions to be executed. A power supply delivers 28V to the testing board through red and black 22 gauge wiring. The location of the power delivery is shown in the diagram below.

Figure 34. PTB Location Power Connectors

c. LM2678 Voltage Regulator

The circuitry has certain constraints in regard to how much power it can handle. Many of the components on the board are not rated for a 28V voltage supply. Therefore, a voltage regulator, a device that functions as a medium to step down voltages to prescribed levels, was needed for the proper operation and protection of the PTB circuitry.

In addition to getting the proper component, Mr. Jordan and the author decided that device needed to be applicable for the scope of the project. The project requires a device that could interface with launch vehicle avionics and be induced into harsh environments. Therefore, as a start, the PTB needs to have the capability to receive at least a 28Vsignal, maintain a high level of efficiency, contain low tolerance percentages, and maintain temperature durability to withstand the temperature environment of the mission.

An LM2678 voltage regulator was implemented to satisfy these requirements. This component is capable of stepping down voltages as high as 40V down to 12V while driving loads up to 5A (LM2678 Simple Switcher High Efficiency 5A Step-Down Voltage Regulator).

Furthermore, the voltage regulator has certain attractive efficiency and tolerance levels. It has a 92% efficiency rating, the output voltage of the device is guaranteed to a $^{+}/_{-}$ 2% tolerance, and the operational temperature range is between -40 to 125^{o}C (LM2678 Simple Switcher High Efficiency 5A Step-Down Voltage Regulator).

The LM2678 device also has built-in protection. It contains a thermal shutdown, current limiting circuitry, and an ON/OFF control input that can reduce the amperage of the device down to 50µA during standby operations (LM2678 Simple Switcher High Efficiency 5A Step-Down Voltage Regulator).

The following diagrams will show the associated cutouts for the schematic and the PTB representations of the LM2678 voltage regulator.

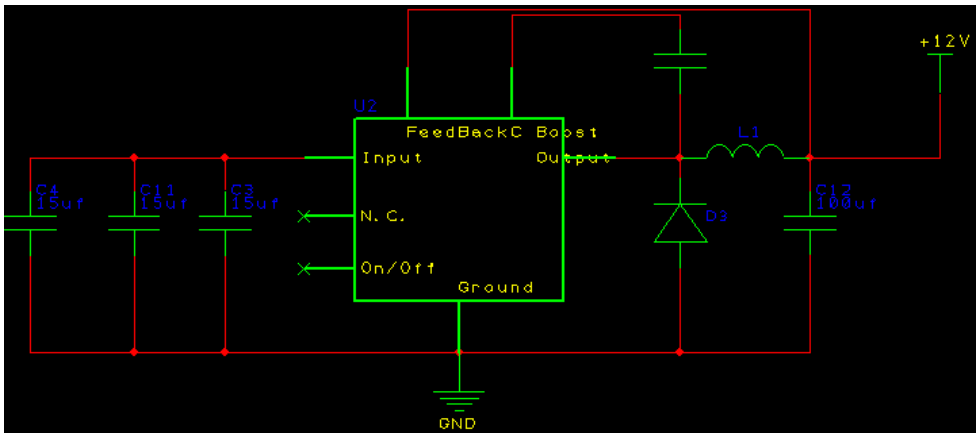


Figure 35. LM2678 Voltage Regulator Schematic Cutout

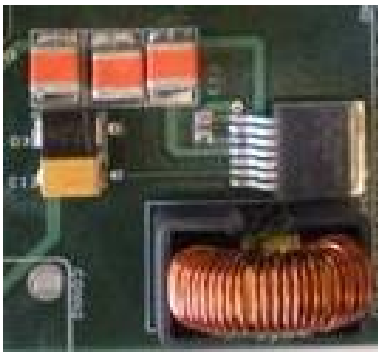


Figure 36. LM2678 Voltage Regulator PTB Cutout

d. Parallax BS2 Basic Stamp Controller

The circuitry is ready to be powered after the voltage regulator steps down the voltage to appropriate levels. Originating at the output of the voltage regulator, the modified power signal travels along the board traces until it arrives at the basic Stamp controller.

The Stamp microcontroller is the “brain” of the entire operation. Without this critical component, none of the command logic could be delivered to the board, none of the electrical components would energize, and the circuit would not fire at the proper sequencing. Samples of the P-Basic programming logic used for testing will be displayed in Appendix G.

Once again, the author and Mr. Jordan used the overarching project criteria to select the appropriate basic Stamp to fit mission requirements. First, the Stamp

had to be compatible with the rest of the PTB components. It must be rated to accept the power signal coming from the voltage regulator. In addition, it must be able to deliver the proper output voltage and current to drive the rest of the circuitry. Finally, it must be able to withstand the temperature extremes of the mission. The actual thermal environment at this point, however, is not defined.

The BS2 module's temperature range is 0^{o}C to 70^{o}C (Basic Stamp Reference Manual Version 2.2). This range is not sufficient to withstand temperature extremes in orbit. Therefore, the author and Mr. Jordan chose the industrial version of the BS2. This version has an environmental temperature tolerance range of -40^{o}C to 85^{o}C (Basic Stamp Reference Manual Version 2.2).

The Stamp accepts between 5.5 to 15VDC on the VIN pin (Basic Stamp Reference Manual Version 2.2). The internal circuitry steps down the 12V output from the voltage regulator to 5V in order to operate other PTB electrical components (Basic Stamp Reference Manual Version 2.2). Finally, the Stamp can accept the programming logic from the basic Stamp editor. Once it has its commands, it can actuate and sequence the PTB circuitry via eight pre-designated pin-outs on the Stamp. The actual output designations of the pin-outs are displayed in the full schematic located in the appendix of this thesis.

e. RS-422 Serial Port Interface and DB-9 Connection

The Stamp must be programmed by an external Stamp editor before the microcontroller can issue commands to the rest of the circuit. This is accomplished by coordinating certain pin-outs on the Stamp with the RS-422 serial port interface and D-sub connection combination that provides a communication link with a PC. The BS2 pin description chart above and the diagram below illustrate the connections between the Stamp and the RS-422 serial port interface.

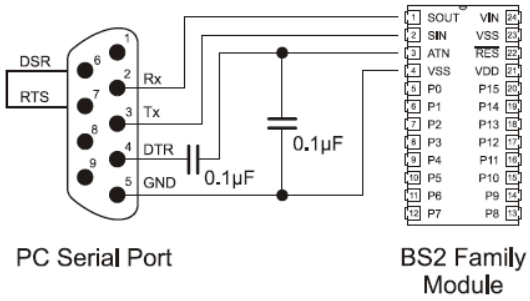


Figure 37. Connection between Stamp and RS-422 Serial Port Interface (From Basic Stamp Reference Manual Version 2.2)

The following diagrams are the representative schematic and PTB illustrations of the RS-422 serial port interface, D-sub female 90^{o} and D-sub male connection, and the circuitry leading to the Stamp controller.

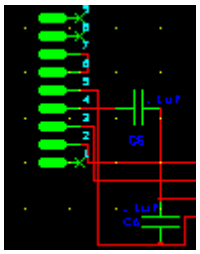


Figure 38. RS-422 Serial Port Interface and Circuitry Schematic Cutout

Figure 39. PTB D-Sub Female 90o Connector and Male D-Sub Cutout

f. Bipolar Junction Transistor (BJT)

The rest of the circuitry is ready to activate now that the Stamp has the proper voltage and communication interfacing. Recall that future versions of the prototype sequencer will have all the necessary components to fire P-POD NEAs.

Furthermore, recall that the current level of development of the prototype sequencer board is a simplified version that only actuates relays in a certain sequence. The actual circuitry that actuates the relays will be discussed at this juncture of the electrical interface discussion. On this note, Mr. Jordan chose several relay drivers to energize the circuit relays. All of them operate in slightly different ways. However, all of them produce the same end result. Once again, the purpose of having these differences in the circuitry is to determine the best products to use for future iterations of the prototype sequencer electrical interface.

The first two types of relay drivers that will be discussed are the transistors. The first kind of transistor that will be discussed is the BJT. There are two BJTs on the PTB. The team chose this device for specific reasons. It is designed for high speed switching using a collector current up to 500mA and a maximum rated voltage of 6V (2N2219/22A High Speed Switches). These properties are suited for the current and voltage capabilities of the Stamp controller. In addition, the BJT has a highly durable temperature range. It can withstand temperatures as cold as -65^{o}C and as hot as 175^{o}C (2N2219/22A High Speed Switches).

Key events take place when the Stamp issues the command through the pin-out associated with this transistor. First the signal is sent along the PTB trace between the designated Stamp pin-out and the transistor. The BJT accepts the low current signal from the Stamp. The BJT triggers and allows the 12V voltage source to provide a high current through the relay circuitry. Inside the relay, the high current originating from the BJT actuation energizes a solenoid to perform further circuitry functions.

The actual solenoid in the diagram below appears to be a part of the BJT as a whole. In contrast, it is not manufactured inside the BJT. It is a separate electrical component that is integrated inside an individual relay.

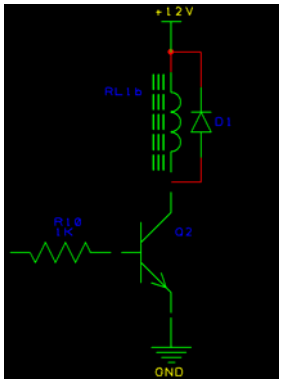


Figure 40. BJT Schematic Cutout

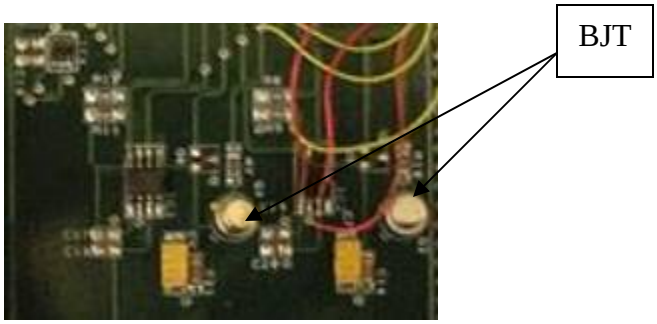


Figure 41. BJT PTB Cutout

g. Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET)

The second type of relay-driving transistor implemented in the PTB is the MOSFET. There are two MOSFETs on the PTB. Similar to the BJT, the MOSFET has an associated pin-out on the Stamp controller. Likewise, when the MOSFET receives the appropriate signal through the associated pin-out, it energizes and actuates an individual relay solenoid. However, unlike the BJT, the MOSFET does not receive a minimal current source (NUD3112 Integrated Relay, Inductive Load Driver). In contrast, it senses an electric field that causes the MOSFET to energize (NUD3112 Integrated Relay, Inductive Load Driver).

Mr. Jordan and the author chose this device for similar criteria as the devices described previously. This device can drive relay coils up to 6W and 12V (NUD3112 Integrated Relay, Inductive Load Driver). The power rating surpasses the minimum power requirements of the Stamp microcontroller making the device ideal for circuit operation. In addition, it can operate at temperatures ranging form -40^{o}C to 85^{o}C

(NUD3112 Integrated Relay, Inductive Load Driver). This temperature range makes the device more suitable to tolerate the harsh environment in space. Below are the schematic and PTB cutouts of the MOSFET.

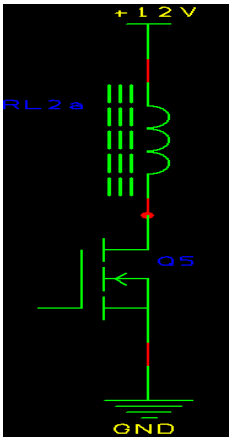


Figure 42. MOSFET Schematic Cutout

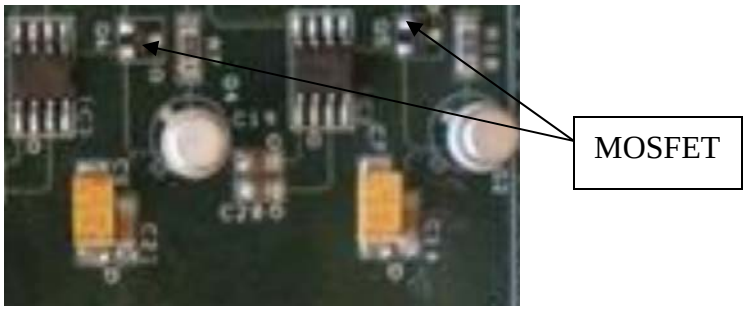


Figure 43. MOSFET PTB Cutout

h. MAXIM 4427 Dual High-Speed MOSFET Drivers

Four additional relay drivers come in two separate dual packages each. The individual package is called the MAXIM 4427 Dual High-Speed MOSFET Drivers. This device receives transistor-transistor logic (TTL) or complementary metal oxide semiconductor (CMOS) inputs to high voltage and current outputs (Maxim Dual High Speed1.5A Mosfet Drivers). Simply put, this device operates similar to two MOSFETs working together to energize two relay solenoids.

Similar to the other previously mentioned descriptions, this device is ideal for the project needs. This device has a 1.5A peak output current to actuate two relays in the PTB (Maxim Dual High Speed1.5A Mosfet Drivers). In addition, its 4.5V to 18V voltage operating range satisfies the 12V relay operating requirement (Maxim Dual High Speed1.5A Mosfet Drivers). It requires low amperages of 1.8mA for logical 1 input and a 200µA logical 0 input (Maxim Dual High Speed1.5A Mosfet Drivers). It has an operating temperature range of -40°C to 85°C. Finally, it offers two protective features. It is latch up protected; meaning, it can withstand 500mA of reverse current. In addition, it is electrostatic discharge (ESD) protected (Maxim Dual High Speed1.5A Mosfet Drivers).

The following diagrams will display the schematic and PTB cutouts of the MAXIM 4427. The solenoids displayed in this diagram are not manufactured inside of the relay driver setup. Rather, they are integrated within their respective relays.

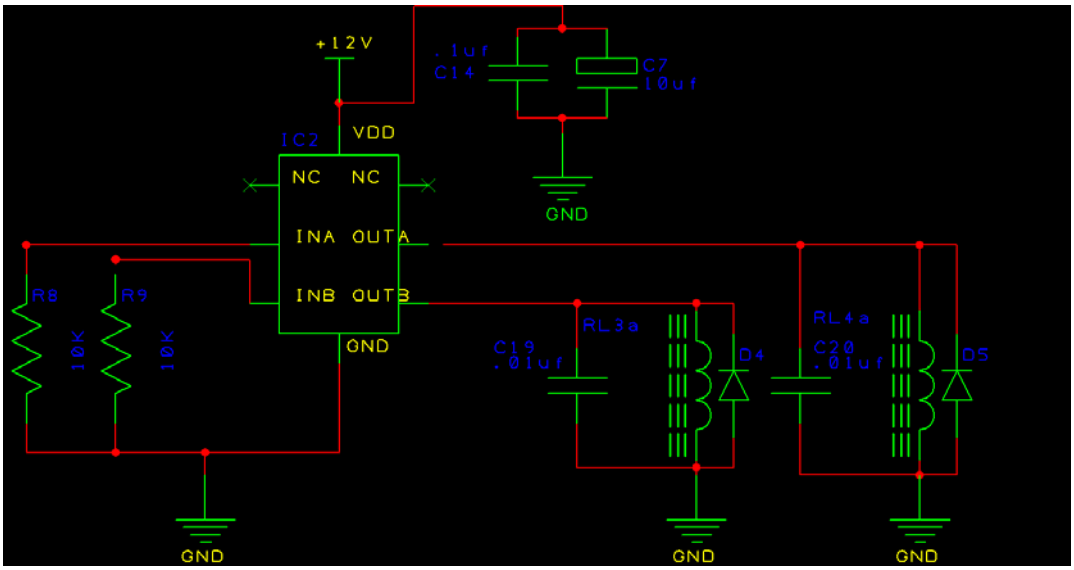


Figure 44. MAXIM 4427 Schematic Cutout

Figure 45. MAXIM 4427 PTB Cutout

i. Relays and Relay Contacts

Finally, the discussion is at the last step of the electrical cycle. As mentioned before, 8 solenoids energize when the 8 relay drivers energize their associated 8 relays. This causes the contacts inside each of the eight relays to close thus allowing 28V 2A power to actuate the P-POD NEAs.

Several different relays are used for the PTB. Once again, the reasoning behind the different components is to determine the best product for future sequencer board iterations. Hence, using different relays follows the same logic. Each relay has similar characteristics. Therefore, only a summary of the common benefits each relay provides will be given. In addition, the author will cite all the respective sources of the relays in the "List of References" section of this thesis. All chosen relays provide high electrical noise immunity, high switching capacity, and a high temperature range (-40^{o}C to 85^{o}C) to fit the needs of the PTB.

Below are the diagram cutouts of the relay contact schematic and PTB. The first diagram illustrates the contact configuration of the eight relays. This illustration does not represent the entire relay circuitry. As mentioned before, these contacts are electrically linked to separate parts of the circuit shown on separate parts of the schematic.

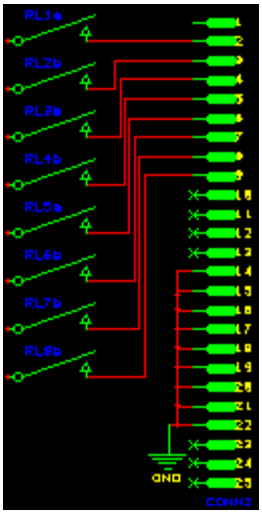


Figure 46. Relay Contact Configuration Schematic Cutout

Figure 47. Relay Contact Configuration PTB Cutout

j. Maxim 6630 Temperature Sensor

The PTB has an adjunct feature to facilitate thermal-vacuum testing. The Maxim 6630 temperature sensor is mounted on the PTB. It has an extended temperature range of -55^{o}C to 150^{o}C (Maxim 12-Bit + Sign Digital Temperature Sensors with Serial Interface). This sensor, along with the Stamp editor and an Excel spreadsheet, will provide temperature indications of the components on the PTB during testing. More discussion of thermal-vacuum testing will be discussed in the following chapter.

The following diagrams are the Maxim 6630 temperature sensor schematic and PTB cutouts.

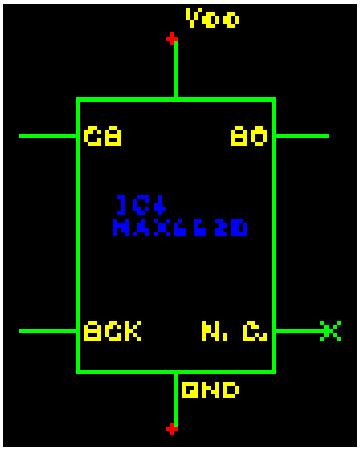


Figure 48. Maxim 6630 Temperature Sensor Schematic Cutout

Figure 49. Maxim 6630 Temperature Sensor PTB Cutout

V. THERMAL-VACUUM TEST

In this chapter, the author details the thermal-vacuum chamber pre-test, proof-of-concept test, and extreme thermal cycle test for the prototype PCB. The purpose of this test is to analyze the behavior of COTS electrical components mounted on the PTB under specified thermal extreme conditions. The Test Requirements for Launch, Upper Stage, and Space Vehicles Volume I: Baselines handbook will be the standard for this testing (MIL-HDBK-340A). Although the testing will be based off this standard, the author will modify the tests accordingly to fit the scope of the thesis.

One pre-test and two one-cycle tests were administered for the testing regimen. The thermal-vacuum chamber pre-test will familiarize the student with the layout of the thermal-vacuum chamber, its associated instruments, and response times of instrument operation. The proof-of-concept thermal cycle test analyzes the electrical components on the PTB based on the most thermally restrictive component. The extreme cycle test examines the electrical components on the PTB based on the least thermally restrictive electrical component.

In all the tests, the author assumes certain values that are based on empirical behavior of the thermal-vacuum chamber. Two temperature meters are located on the thermal-vacuum chamber. There are thermocouples inside of the chamber that connect to a display outside the chamber. In addition, there is a temperature meter that is associated with the temperature of the inner shell of the chamber. Considering that the test will be conducted in a vacuum, the conduction of heat will likely be the predominant form of heat transfer overriding radiation coupling. On this note, the PTB may not follow the same temperature trends as the temperature indications.

The testing follows the procedures specified in the "NPSCuL-Lite Prototype Sequencer Electrical Board Unit Thermal Acceptance Test" located in the final appendix of this thesis. Furthermore, information concerning procedures, military specification standards, equipment lists, and requirements are elaborated in this document. Before the three tests were conducted, the author researched the capabilities of the thermal-vacuum chamber and created expected temperature profiles for each test. Creating expected

profiles is a good practice because it gives the examiner guidelines for testing. For all the following tests, the author will compare and contrast the expected data versus the actual data. Furthermore, the author will detail modifications from the expected test procedure and explain how that may have affected the actual test results.

A. THERMAL-VACUUM CHAMBER PRE-TEST

1. Expected Thermal-Vacuum Chamber Pre-Test

At the time this test was being conducted, some of the operational parameters of the thermal-vacuum chamber were not entirely known. However, the author did know that the chamber has certain heat up/cool down empirical characteristics. During previously conducted tests, the thermal-vacuum chamber exhibited heat up rates that are similar to MIL-HDBK-340A standards. This value is 3^{o}C to 5^{o}C per minute (MIL-HDBK-340A). Additionally, the cool down rate of the chamber was proven to be < $^{1}/_{10}{}^{o}$C per minute in previous tests (Phelps). These values are implemented in the calculations of each stage duration. Additionally, these durations are expressed in the following expected thermal-vacuum chamber pre-test table.

The following table and chart depict the expected thermal-vacuum chamber pre-test. The temperature and duration values associated with the different phases displayed in this table are not within military specification. The values do not need to be congruent with military specification considering that this test is simply an operational verification of the thermal-vacuum chamber.

Thermal-Vacuum Chamber Pre-Test with Vacuum			
Phase	**Temperature (^{o}C)**	**Duration (minutes)**	**Accumulated Time (minutes)**
Ambient to Cold Soak	23 to 8	151	151
Temperature Stabilization Cold	8	6	157
Cold Soak	8	10	167
Transition to Hot Soak	8 to 43	13	180
Temperature Stabilization Hot	43	6	186
Hot Soak	43	10	196
Transition to Ambient	43 to 23	201	397

Total Cycle Testing Time
6 hours 36 minutes

Table 9. Expected Thermal-Vacuum Chamber Pre-Test Cycle Description Table

The following graph is the associated graph for the thermal-vacuum chamber pre-test. Note the steady linear declining slopes and the rapidly rising positive slope. These slopes are associated with the expected cool down and heat up rates, respectively. The momentary plateaus in the curve illuminate the temperature stabilization and soaking periods.

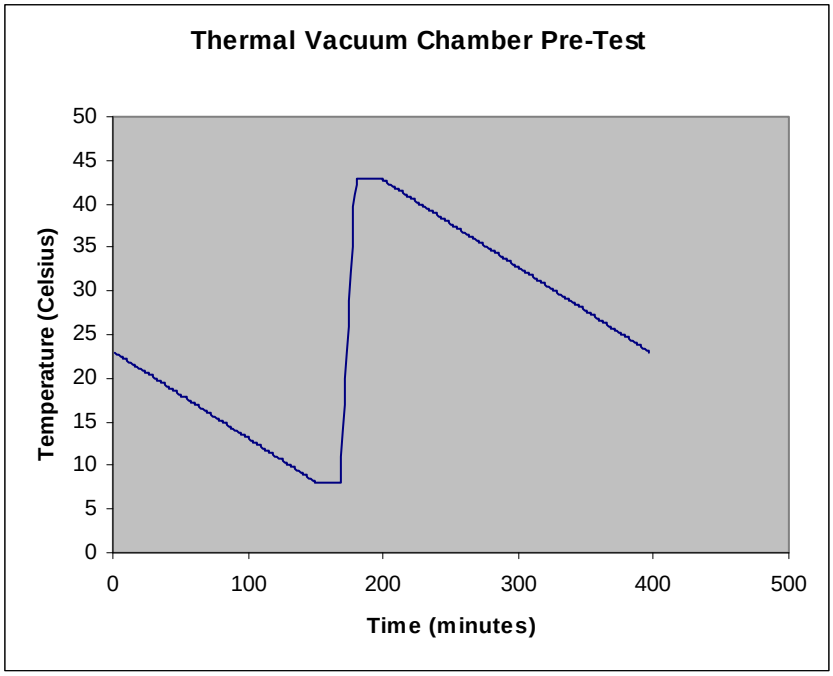


Figure 50. Expected Thermal-Vacuum Chamber Pre-Test Graph

2. Actual Thermal-Vacuum Chamber Pre-Test

The conducted pre-test contains some contrasting features when compared to the expected values. First the temperature and duration requirements change. Instead of starting at the expected ambient temperature of 23^{o}C, the test started at 18^{o}C. In regard to duration, the actual test was significantly different than the predicted values. Each stage had different durations, with the exception of the cold temperature stabilization phase. One reason for this is that cooling down the chamber took a nominal 1^{o}C per minute cool down rate. This value was ten times greater than what was expected. Thus, cooling down the chamber took significantly less time than expected. Another reason was that the examiner was getting accustomed to the controls and overall operation of the vacuum chamber. In fact, the cool down rate could have been even greater in magnitude if the

author had been familiarized with the system. Likewise, the overall duration of the test is significantly less than the expected overall duration due to the greater cool down rate.

Other reasons exist for the aberration of actual duration values. One reason is that the operator did not let the chamber dwell at the specified temperatures at the appropriate times. To illustrate, the cold soaking period should have been ten minutes long. The actual test has only a seven minute long dwell time. Likewise, the hot stabilization and soak periods demonstrate the same aberration.

Furthermore, the transition to the hot soak phase has a divergent value. This error did not occur because of equipment operational capabilities. This error occurred because of operator error. During the transition period to hot soak, the examiner failed to set the TempTenn control setpoint to 53^{o}C until the shell temperature of the chamber was at 33^{o}C. The setpoint should have been adjusted before the transition to the hot soak phase. This caused an abnormally long dwell at this temperature and slowed the rate of heating to approximately 0.9^{o}C per minute. Consequently, this prolonged the transition to the hot phase and added more time to the entire procedure.

The following table depicts the actual thermal-vacuum chamber pre-test.

Thermal-Vacuum Chamber Pre-Test (Vacuum)			
Phase	**Temperature (oC)**	**Duration (minutes)**	**Accumulated Time (minutes)**
Ambient to Hot Soak	18 to 8	23	23
Temperature Stabilization Cold	8	6	29
Cold Soak	8	7	36
Transition to Hot Soak	8 to 43	39	75
Temperature Stabilization Hot	43	3	78
Hot Soak	43	5	83
Transition to Ambient	43 to 23	26	109

Total Cycle Testing Time
1 hour 49 minutes

Table 10. Actual Thermal-Vacuum Chamber Pre-Test Description Table

The following graph has the overall shape of the expected value curve. However, it has some distinctions. First, note the initial plateau at 18^{o}C. When the test commenced, the actual cool down process took 15 minutes to initiate. Therefore, the

temperature remained at a steady 18°C. In addition, the initial cool down rate was much steeper than expected as explained previously. Finally, the graph illuminates the flatter slope representing the 0.9°C per minute heat up rate. Once again, this rate caused the phase duration to increase and diverge from the expected value.

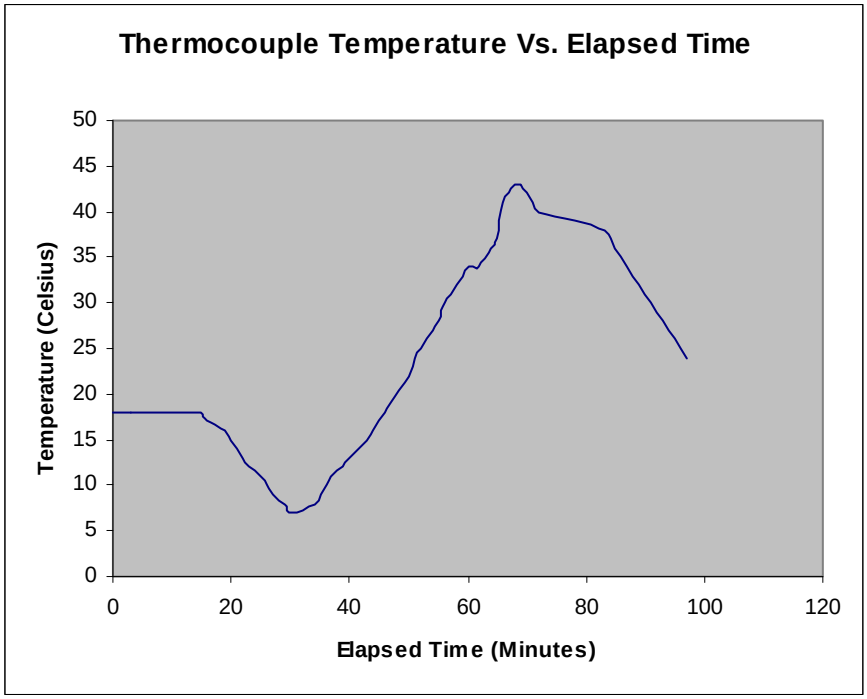


Figure 51. Thermocouple Temperature vs. Elapsed Time Graph

There are two different temperature indications on the thermal-vacuum chamber. The thermocouple thermometer displays temperatures of the different thermocouple leads inside the chamber. This temperature is the primary temperature being monitored and analyzed for testing purposes during the pre-test. The TempTenn temperature display delivers temperature readings on the internal shell temperature of the thermal-vacuum chamber.

The temperature is monitored for certain reasons. First, the operator uses the TempTenn instrument to manipulate temperature setpoints. These setpoints will indirectly determine the thermocouple temperature in the vacuum chamber. Second, the TempTenn instrument is used to control heat up and cool down rates of the internal shell temperature. Once again, this control will indirectly affect the temperature, heat up and

cool down rates of the thermocouples. Since the pre-test is primarily for operator familiarization, this temperature reading will only be discussed during the pre-test section of the testing procedure.

During the pretest, the examiner noticed certain trends with the shell temperature. First, the shell temperature seemed to lead the thermocouple temperature by approximately 10^{o}C with the exception of the peaks of the curves. At the peaks, the lead-lag behavior between both detectors initially swaps, and then they arrive at an equilibrium. Finally, the expected behaviors between both detectors return to normal.

The heat up and cool down rates of the shell temperature are more extreme than the same rates for the thermocouples. For the first cool down transition, the cool down rate averaged at approximately 1.5^{o}C per minute. The heat up rate averaged at approximately 1.7^{o}C per minute. And, the final transition to ambient temperature cool down rate averaged at approximately 2.7^{o}C per minute. This final cool down rate is higher than the initial cool down rate. The reason for this occurrence is that the thermal-vacuum chamber instrumentation is stabilized during the last phase and can respond more rapidly to instrument manipulation. Whereas, the initial cool down rate is not operating under stabilized conditions.

There is one final difference between the thermocouple and shell temperature indications. Recall that the thermocouple indications dwell for a specific period of time at the cold and hot stabilization and soak phases. In contrast, the shell temperatures do not dwell at these peaks. Since the shell temperatures indirectly determine thermocouple temperature, they have to be adjusted consistently in order to keep the thermocouple temperatures in the proper bands. Therefore, these temperatures do not have any relatively long durations at any specific temperature. Furthermore, the purpose of this test is not to test shell temperature reactions. Hence, the shell temperature does not have to follow the pre-test profile.

The following graph shows the shell temperature versus elapsed time curve.

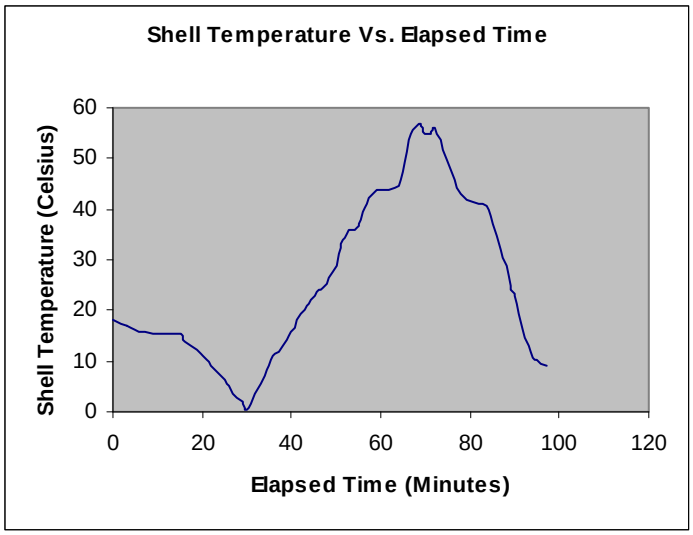


Figure 52. Shell Temperature vs. Elapsed Time

3. Thermal-Vacuum Chamber Pre-Test Conclusions

The pre-test of the thermal-vacuum chamber provided decisive conclusions. First, the author severely underestimated the cool down rates of the thermal-vacuum chamber. The pre-test shows that the chamber is capable of cooling down at rates that meet the military specification. However, cooling down the actual PTB may be a different case. Recall that the pre-test simply measured the temperatures of the thermocouples and the shell chamber wall. Furthermore, the temperature sensor on the PTB will provide the reference temperature for the board itself. So, the temperature of the chamber could be a certain value and the temperature of the PTB could be a completely different value. In other words, the PTB could be lagging or leading any of the thermocouple and/or shell temperatures. In addition, the PTB could be lagging or leading in respect to the heat up and cool down rates. Therefore, in order to mitigate unexpected scheduling and temperature profiling issues, the author will maintain the same conservative expected cool down and heat up rates used for the pre-test for the rest of the testing cycles. These rates will be used until further relevant information about the board is revealed during the proof-of-concept test.

Second, the examiner will operate the chamber in a more effective manner. As mentioned previously, the author failed to manipulate the chamber instruments correctly.

This caused abnormally slow heat up and cool down rates. Consequently, this failure also caused stage duration times to be abnormal as well. These abnormalities will be alleviated now that the author has familiarity with the system.

In addition, the author learned that the TempTenn monitor should be 10oC lagging or leading the thermocouple reading for cool down and heat up rates respectively. As a result, the respective rates can cool or heat the chamber in a more time efficient manner. Thus, the test could more precisely reflect the regulations of MIL-HDBK-340A.

B. PROOF-OF-CONCEPT THERMAL CYCLE TEST

1. Expected Proof-of-Concept Thermal Cycle Test

The proof-of-concept test is administered to verify the manufacturer's specification on certain electrical components. In this testing, the author based the temperature ranges on the most thermally sensitive temperature component on the PTB. In other words, the temperature components that have the lowest maximum temperature and the highest minimum temperature are used as the baseline proof-of-concept temperature extremes for this testing cycle. The temperature range that the examiner uses is -40^{o}C to 85^{o}C. This temperature range is based on the thermal operational characteristics of the J-SM1 relay, the JQ-1 relay and the JW5 relay driver. Further detailed information concerning components and temperature ranges are detailed in the testing document at the end of this thesis.

There are reasons behind testing the thermal components referencing the most thermally restrictive component. First, the author wants to see if the board can handle extreme temperatures at the lowest temperature operating range. If the PTB passes this test, then the electrical board can undergo more severe testing in the future. Another reason why the author chose this temperature range is that the examiners do not wish to break the board in this cycle. Once again, the whole point of this test is to see if the electrical components of the board can function in the manner in which the manufacturers claim they can perform. Hence, breaking the board at this stage is not appropriate. The job of breaking the board is left to the extreme thermal cycle test.

Once again, the proof-of-concept thermal test was conducted based on military specifications. Considering the capabilities of the thermal-vacuum chamber, the test is not expected to meet the criteria delineated in the MIL-HDBK-340A. Therefore, the test is modified to meet the examiners scope of the testing. Based on pre-test results, the same phase durations, cool down rates, and heat up rates are applied for this phase of testing.

The following table and graph summarize the expected duration and phase temperatures of the proof-of-concept thermal cycle test.

Proof-of-Concept Cycle with Vacuum			
Phase	**Temperature (^{o}C)**	**Duration (minutes)**	**Accumulated Time (minutes)**
Ambient to Hot Soak	23 to 85	22	22
Temperature Stabilization Hot	85	30	52
Hot Soak	85	60	112
Transition to Cold Soak	85 to -40	1251	1363
Temperature Stabilization Cold	-40	30	1393
Cold Soak	-40	60	1453
Transition to Ambient	-40 to 23	22	1475

Total Cycle Testing Time
24 hours 35 minutes

Table 11. Expected Proof-of-Concept Thermal Cycle Test Description Table

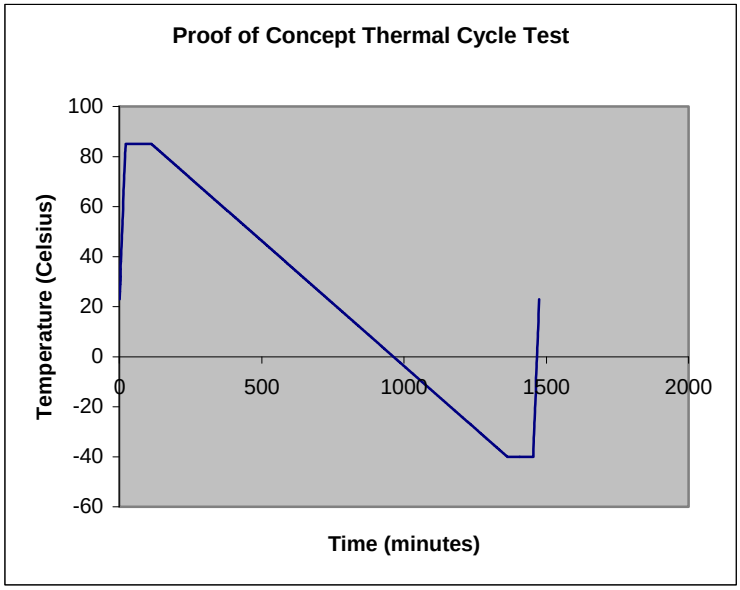


Figure 53. Expected Proof-of-Concept Thermal Cycle Test Graph

2. Actual Proof-of-Concept Thermal Cycle Test (Hot Phase)

The heating and cooling of the chamber and internal components performed as expected from the pre-test. The chamber shell temperature always leaded in heating and cooling in respect to the thermocouple temperature indicator and the temperature sensor of the board. Furthermore, the thermocouple temperature always led in heating and cooling relative to the temperature sensor mounted on the PTB. The amount that each component's temperature led another varied over the course of testing. Furthermore, in order to keep the temperature sensor in the proper temperature band, all of the heating and cooling instrumentation had to be used on a consistent basis. This may show that the thermal-vacuum chamber can not maintain temperatures at a certain level for long periods of time. Moreover, this shows that the thermal-vacuum chamber requires constant monitoring.

Tables and graphs will not be displayed in this section for the chamber shell and thermocouple temperature indications. The behavioral characteristics of each indication are discussed in the pre-test section above. The author manipulated each of the indications to provide the proper temperature band for the PTB.

In addition, other performance expectations were reaffirmed during this testing. First the heat up rate of the chamber performed as expected. The chamber heated up at an average of 1.35^{o}C per minute. This is similar to the expected 1.7^{o}C rate given by the pre-test. Furthermore, the pre-test concluded that the thermal-vacuum chamber's cool down rates were significantly underestimated. The conclusion stated that there is a chance that the cool down duration of each cool down transition, as well as the entire overall cycle duration, will be significantly reduced if the pre-test results were accurate. The test shows great confidence that the chamber can provide cool down rates faster than $^{1}/_{10}$ ^{o}C per minute. In fact, the PTB cooled down at a little over 1^{o}C per minute. This is a significant improvement over what was initially expected. Consequently, testing durations for each phase and the overall test was reduced.

However, an anomaly occurred during the testing that terminated the proof-of-concept test prematurely. The PTB and communications board configuration failed 3 hours and 14 minutes into the proof-of-concept test. A communications error between the master communications microcontroller and the slave communications microcontroller in the chamber caused the PTB to stop its sequence and temperature indications. The last recorded reading before the failure occurred when the chamber was transitioning to cold soak at the above mentioned time at 26^{o}C. The board was inoperative when the author attempted to restart the PTB setup several times during the testing cycle.

After the entire system shut down for a day and all conditions returned to normal, the author attempted to restart the system and verify the status of its operation. The PTB worked properly. Further testing will be done considering that the PTB is operational.

The following table and graph illustrates the shortened proof-of-concept thermal cycle. Due to the premature test termination, the test only includes a transition from ambient to hot soak phase, hot temperature stabilization phase, hot soak phase, and a partial transition to cold soak phase.

PTB Temperature Sensor Proof-of-Concept Cycle with Vacuum (Hot Phase)			
Phase	Temperature (^{o}C)	Duration (minutes)	Accumulated Time (minutes)
Ambient to Hot Soak	23 to 85	46	46
Temperature Stabilization Hot	85	30	76
Hot Soak	85	60	136
Transition to Cold Soak	85 to 26	58	194

Total Cycle Testing Time
3 hours 14 minutes

Table 12. PTB Temperature Sensor Proof-of-Concept (Hot Phase) Table

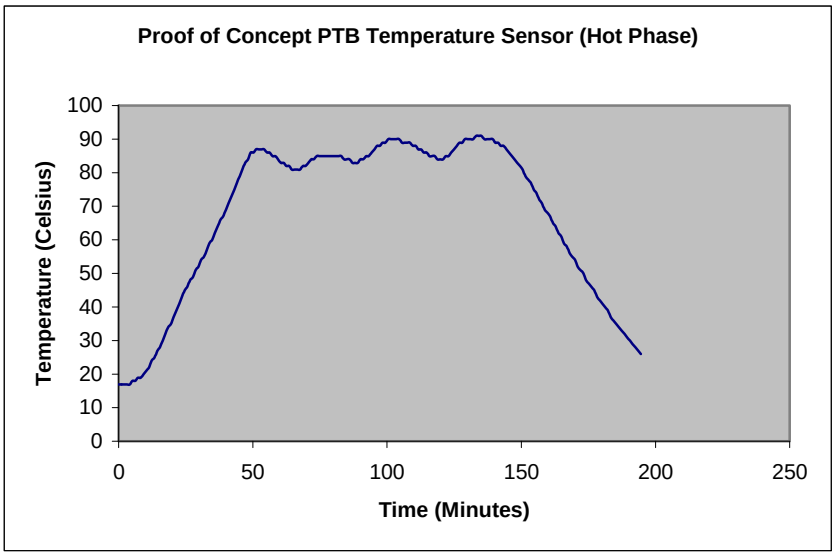


Figure 54. Actual Proof-of-Concept Temperature Sensor Graph

3. Proof-of-Concept Thermal Cycle Test Conclusions

All in all, the proof-of-concept thermal cycle test provides several results. First, it reaffirms the author's analysis and conclusions of the pre-test. Second, the author will change the expected heat up and cool down rates of the extreme thermal cycle testing to match the empirically proved results from the pre-test and the proof-of-concept test. Third, the anomaly may provide substantial results in further phases of testing and will be investigated further.

a. Troubleshooting Reveals Cause of Failure

Although the above theories seem feasible, they are not founded on concrete evidence. After the failure, the author and Mr. Jordan troubleshot the circuitry to reveal the discrepancy. The investigation brings up several key points.

One point deals with the communication configuration with the communication board, the PTB, and the PC. The interface is set up in a master-slave configuration. The following process illustrates the inner workings of this configuration. The examiner types in an algorithm on a Stamp editor installed on PC. This algorithm gets programmed on the microcontroller situated on the communication board via a D-sub connector. Once the master microcontroller receives the appropriate signal, it will interface with the slave controller mounted on the PTB. The master will command the slave to run through the program sequence, actuate associated relays, and feedback certain information. The slave will feed back an indication stating that a specific relay actuated and a temperature reading of the PTB. Once the communication board receives this information, it delivers this information to the PC for examiner records and analysis.

If the communication interface between both microcontrollers fails, the slave controller can not perform its sequence, the master microcontroller stops issuing commands and delivers an error signal, and finally, the PC will stop receiving and storing data. This failure occurred during the proof-of-concept testing. Thus, the cycle ended prematurely.

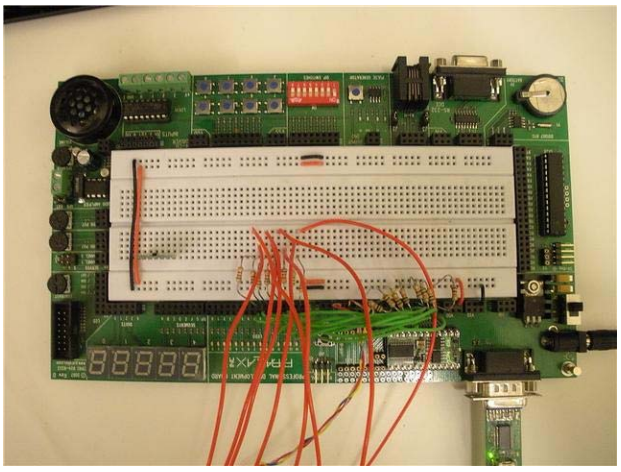


Figure 55. Communication Board

All in all, this cycle of testing was terminated prematurely and the author will move on to the final stage of testing. The test shows that the components withstood the transition to 85^{o}C temperature extreme including the temperature stabilization and hot soak phases. However, the internal circuitry did not function during the cool down to the cold extreme of the cycle. Considering the results of this test, the author will be especially wary of component failures during the final cycle cool down.

In addition, certain modifications to the communication configuration will be implemented to facilitate proper operation of the PTB during the extreme thermal cycle test. Considering that the PTB can be programmed to operate autonomously, the examiners will terminate the use of the communication board as a master controller and allow the PTB to run autonomously. The communication board will be utilized as a voltage divider to allow for relay firing indication via the LED configuration integrated on the communication board.

C. EXTREME THERMAL CYCLE TEST

1. Expected Extreme Thermal Cycle Test

The extreme thermal cycle test's purpose is to push the PTB circuitry to thermal failure. In this testing, the author based the temperature ranges on the least thermally sensitive temperature component on the PTB. In other words, the temperature components that have the highest maximum temperature and the lowest minimum temperature are used as the baseline proof-of-concept temperature extremes for this testing cycle. The temperature range that the examiner uses is -65^{o}C to 175^{o}C. This temperature range is based on the thermal storage characteristics of the 2N2222A NPN Transistor. Further detailed information concerning components and temperature ranges are detailed in the testing document at the end of this thesis.

There are reasons behind testing the thermal components referencing the least thermally restrictive component. First, the author already verified that the board does work at a proof-of-concept hot soak conditions. The only data that is missing in that testing cycle is the proof-of-concept cold soak conditions. Thus, the author decides to add a cold soak at -40^{o}C in the extreme cycle testing in order to get the proof-of-concept

data. Aside from this special condition, there is little need to determine if the components would work at the proof-of-concept temperature range all over again. Therefore, it is appropriate to push the circuitry to maximum temperatures or until failure.

Another reason for the severity of this testing is for the purposes of creating a more capable electrical board in the future. As mentioned before, the PTB has specific purposes. One, it simulates the opening sequence of 8 P-PODs. Another purpose is that it is used for testing COTS products. Once the appropriate testing is done for these products, the author will filter out the components that survived the tests and implement the same models of those components in future iterations of the prototype sequencer board. The resultant product will be a flight capable electrical interface with test proven products.

Once again, the extreme thermal test was conducted based on military specifications. Considering the capabilities of the thermal-vacuum chamber, the test is not expected to meet the criteria delineated in the MIL-HDBK-340A. Therefore, the test is modified to meet the examiners scope of the testing. Based on pre-test results, the same phase durations, cool down rates, and heat up rates are applied for this phase of testing.

The following table and graph summarize the expected duration and phase temperatures of the expected extreme thermal cycle test.

Extreme Cycle with Vacuum			
Phase	**Temperature (°C)**	**Duration (minutes)**	**Accumulated Time (minutes)**
Ambient to Hot Soak	23 to 175	52	52
Temperature Stabilization Hot	175	30	82
Hot Soak	175	60	142
Transition to Cold Soak	175 to -65	2401	2543
Temperature Stabilization Cold	-65	30	2573
Cold Soak	-65	60	2633
Transition to Ambient	-65 to 23	31	2664

Total Cycle Testing Time
44 hours 24 minutes

Table 13. Expected Extreme Thermal Cycle Test Description Table

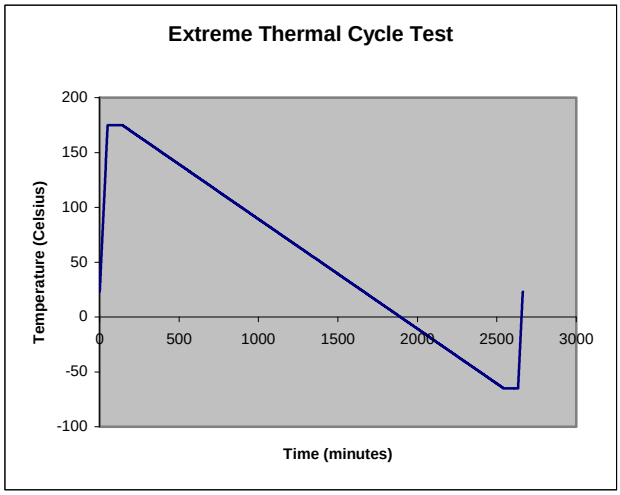


Figure 56. Expected Extreme Thermal Cycle Test Graph

2. Actual Extreme Thermal Cycle Test

Before the actual extreme thermal cycle test commenced, the author implemented a change from the expected thermal profile. As mentioned in the previous section, the author chose to use part of this test to capture proof-of-concept cold soak data. Typically, these tests start with a transition to a hot soak. Considering that the purpose of this test is to break the electrical interface, bringing the board all the way up to a 175°C hot soak

would cause the board to shut down. Moreover, in a worst case scenario, this temperature could possibly permanently warp the board thus making it impossible to function properly. Therefore, bringing the board down to a cold soak is the best course of action in order to get the proper cold soak data, to not irreparably damage the board, and to get a full cycle of data.

During the transition to cold soak, earlier empirical results were reaffirmed and new information was revealed in regard to the thermal-vacuum chamber. As mentioned previously, the cool down temperature rate for the thermal-vacuum chamber is $^{1}/_{10}{}^{o}$C per minute. The chamber achieved this rate once it breached a cold temperature threshold of -29^{o}C.

The following table illuminates the cool down rate characteristics of specified cold temperature bands.

Temperature (^{o}C)	Cool Down Rate (^{o}C/min)
Ambient to -10	0.5
-11 to -16	0.33
-17 to -20	0.25
-21 to-23	0.2
-24 to -27	0.13
-29 and colder	.1 or less

Table 14. Cool Down Rates of Cold Temperature Ranges

As the temperature dropped lower than -29^{o}C, the cool down rate continued to diminish. At -39^{o}C, the temperature of the board virtually remained fixed at that value. The shell and thermocouple indications also showed fixed values of -78^{o}C and -45^{o}C respectively. If given enough time, the board would have eventually cooled to these values. However, time was limited and the chamber coolers could not physically cool down the chamber shell any more than the existing temperatures. Consequently, as time continues during the cool down, the harder it becomes to lower the temperature of the PTB. Considering the student's time constraints and the functional capacity of the thermal-vacuum chamber, the author decided to commence a cold soak at this temperature to fulfill the proof-of-concept requirements; and, once the cold soak was finished, the board began its transition up to a hot soak.

The board transitioned to a hot soak with an approximate 2°C per minute heat up rate. Once the board temperature reached 118°C, the PTB sequencing process terminated abruptly. Failing at this temperature is expected considering that certain components have operational thermal maximums at 85°C. However, further investigation into the failure reveals an anomaly that was not expected. This will be detailed more in depth in the following section.

The following table and graph illustrates the shortened extreme thermal cycle. Due to time, functional capacity of the chamber, and premature test termination, the test only includes a transition from ambient to cold soak phase, cold temperature stabilization phase, cold soak phase, and a partial transition to a hot soak phase.

PTB Temperature Sensor Proof-of-Concept Cycle with Vacuum (Hot Phase)			
Phase	Temperature (°C)	Duration (minutes)	Accumulated Time (minutes)
Ambient to Cold Soak	23 to -39	249	249
Temperature Stabilization Cold	-39	30	279
Cold Soak	-39	60	339
Transition to Hot Soak	-39 to 118	99	438

Total Cycle Testing Time
7 hours 18 minutes

Table 15. Actual Extreme Thermal Cycle Test Table

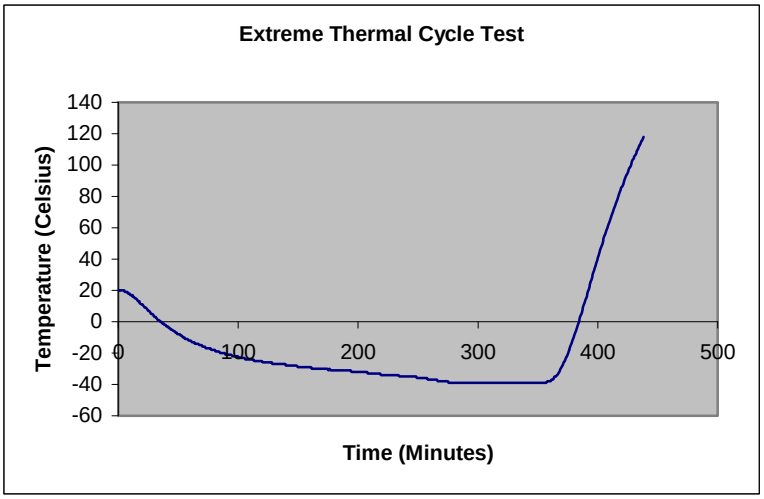


Figure 57. Actual Extreme Thermal Cycle Test Graph

3. Extreme Thermal Cycle Test Conclusions

Before actual troubleshooting was administered, the examiners had an idea where the anomaly occurred. Once the 118^{o}C temperature level was reached, certain indications revealed the source of the problem. The LED indications on the communications board stopped lighting up. This reveals that the PTB relays stopped firing. Furthermore, the data stopped populating on the PC. This evidence suggests that the Stamp stopped working. Considering these two indications, the examiners determined that the Stamp stopped functioning at 118^{o}C thus causing the rest of the circuit to shut off.

This conclusion was not final. The examiners hypothesize that the Stamp could be the likely culprit that caused the board failure. On the other hand, the Stamp could very well have not malfunctioned during testing. Rather, a component upstream of the Stamp could have malfunctioned which caused the Stamp to become inoperative. After some preliminary troubleshooting, the examiners concluded that it is in fact a component upstream of the Stamp that malfunctioned. This component was determined to be associated with the voltage regulator.

Detailed troubleshooting reveals certain things about the malfunction. One, it was not the voltage regulator unit that failed. In contrast, it was a protection diode connected to the output of the voltage regulator that failed. Specifically, this component is suspected to have shorted out at 118^{o}C. When it shorted, 12V output of the voltage regulator could not be supplied to the rest of the circuit. Instead, this output was shorted to ground causing the rest of the PTB components to go dead.

The following illustrations show the voltage regulator circuit including the faulty diode.

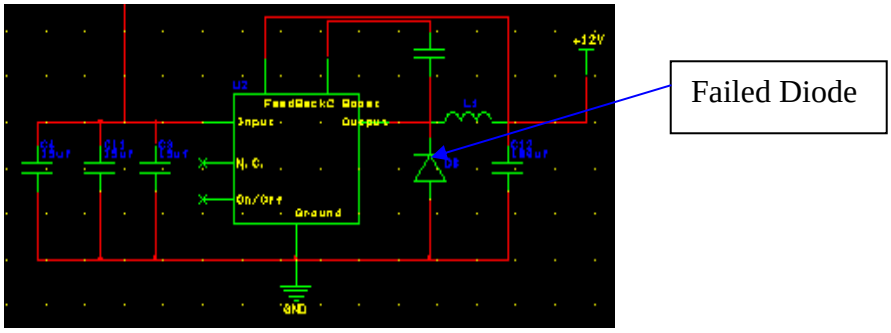


Figure 58. Failed Diode Schematic Cutout

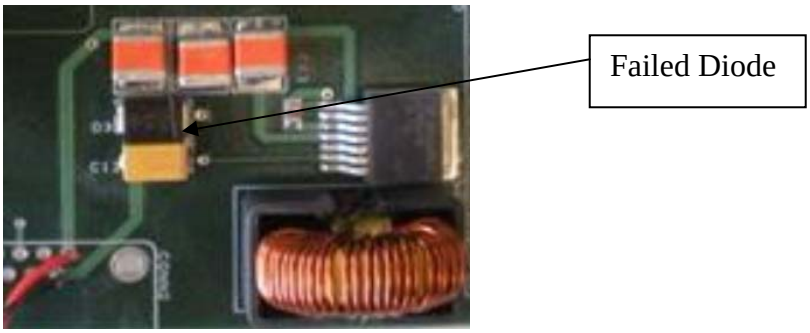


Figure 59. Failed Diode PTB Cutout

VI. CONCLUSION AND POSSIBLE FUTURE WORK

A. PROJECT CONCLUSION

The CubeSat community has grown leaps and bounds since the early 1990s. In this period of proliferation, CubeSats have gained a level of sophistication that is equivalent to many of their large satellite predecessors. Currently, several global communities from several disciplines enjoy the benefits that CubeSats have to offer. In fact, international entities are leveraging CubeSat technology and emerging as global space powers. In regard to this nation's security, this fact may pose certain threats to the U.S.

NPS is among the many professional institutions worldwide who are reaping the benefits of CubeSat technology. Specifically, the school has employed CubeSat technology in several local programs, including the NPSCuL-Lite program. Being part of the NPSCuL-Lite project, the author's prototype sequencer has added utility to the overall project and mission. Moreover, the team gained valuable insight and learning in a professional engineering project. The team witnessed firsthand the dynamic nature of project scheduling and budgets. For example, the author became aware during the development of the thesis that the individual's project development depends heavily on external partners. If an external entity's schedule changes, most likely this change will affect an individual's work, as well.

In addition, the author learned that travel costs can be the majority of the expenditures in a school-hosted engineering project. Therefore, preemptive measures should be taken early in the project development to mitigate this issue.

In regard to the specifics of the author's thesis, several issues still remain to be investigated. For example, the CG placement of the prototype sequencer needs to be within allowable limits in respect to ULA specifications. Furthermore, mechanical mass and final models, with proper feature sizing and placement, need to be machined for further testing and analysis.

In respect to the electrical portion of the thesis, several issues still remain to be reviewed. Although a functional test board was created, an actual flight-like electrical interface is required for further stages of the project development. This development would also include the appropriate testing as well.

The NPSCuL-Lite project as a whole has evolved from talks at a conference in Logan, UT into ADamSat, to what will have to be a million dollar plus funded, widely collaborative, and multi-disciplinary project (Newman et al). This overall project, including the prototype sequencer, will employ new students and focus their respective research until the L41 launch next year (Newman et al). Once NPSCuL-Lite, is successfully launched, it will provide an unparalleled CubeSat launch capacity. Morevoer, NPSCuL-Lite may also eventually help university CubeSat developers get rides for their CubeSats as well.

B. POSSIBLE FUTURE WORK

1. Testing

The focus of this section is not to belabor testing analysis, procedures, documentation, and results. However, the author did attempt to generally apply each of the above testing practices to provide more of a complete thesis. A future student could possibly continue the author's work by making the emphasis of his thesis on the detailed testing of the prototype sequencer.

a. Functional, Vibration, Shock, Thermal, and Vacuum Testing

A student could provide a detailed analysis for the prototype, if he conducts these testing regimes. Sine sweep, random vibration, and shock testing would not only be a good learning experience for the student, but it would also provide a preliminary foundation of what is required for flight unit acceptance testing. This is especially important if NPS is ever charged to deliver a flight capable sequencer. The school would need documentation on the testing processes to deliver a flight ready sequencer.

b. PCB Resonant Frequency and Component Placement

In addition, a student could provide an in-depth analysis of resonant frequencies of PCBs and associated resonant frequency mitigation techniques. One of the key issues in PCB testing is whether or not the PCB can withstand the rigors of a satellite launch. The student could research the vibration characteristics of a PCB and the associated electronic components embedded on the board. Then he could accurately place the components on a board that would provide the optimum function and stability.

c. RF Hardening

Another topic that a future student may want to explore is RF Hardening. The sequencer will be subject to several electromagnetic interactions, as it is being launched and when it is orbiting. One of the various tests that could be performed is an RF test. A future student could research and conduct a test on the sequencer that would illustrate the sequencer's performance before and after being induced in a heavy RF environment. From the test results, the researcher could then propose a system that would be best suited for the NPSCuL-Lite Sequencer.

2. Qualified Flight Article Sequencer

The purpose of this thesis project was to create a "flight-like" sequencer. This implies that it will not have all the necessary characteristics to be flown in space. On that note, a future student could use this thesis as a launching off point for the development of an in house sequencer that is fully qualified to fly in space.

a. Developing the Primary Test Board

A future student may wish to further develop the primary test board. Simply put, the primary test board was made to test the electrical components that were mounted on the board. Recall that the purpose of the PTB was to test the electrical components mounted on the board for thermal-vacuum testing. Therefore, the board was loosely developed to reflect the FRD that specifies what a flight-like qualification

prototype sequencer would exhibit. A future student could expand this work, using the primary test board as a foundation, and develop a flight-like sequencer using the same test proven components of this thesis.

b. Sequencer Integration

The progress of this thesis includes the creation of fundamental mechanical and electrical designs of a prototype sequencer. The author described the creation processes for each, the functioning attributes of each, the level of fidelity of each, and accompanying documents that provide further detail and analysis of the mechanical and electrical designs. In addition to further testing, the prototype sequencer needs to be integrated electrically and mechanically into one integrated unit. A student could take this as at least a part of his work and develop a procedural document and the necessary specifications of work needed to create an integrated complete prototype sequencer. Furthermore, once the integrated sequencer is constructed, the student could write another procedural document, develop the necessary specifications and perform the additional necessary tasks to integrate it with the NPSCuL-Lite structure.

3. Component Research

This thesis was created within the appropriate guidelines of a space systems operations student. Although the entire project involved many elements from various engineering disciplines, the majority of the work and research did not delve to the level required for an engineering thesis. A future student could take the work done for this thesis and provide further detailed analysis on each of the components on an engineering level. This work could illuminate more possibilities, understanding, and create a higher quality product with increased fidelity.

LIST OF REFERENCES

"2N2219/22A High Speed Switches." E-mail sent to the author. STMicroelectronics, 2003. Naval Postgraduate School, Monterey. 1 Apr. 2009.

Basic Stamp Syntax and Reference Manual Version 2.2. Parallax Inc., 2005. 1 Jul. 2008. <http://www.parallax.com>

Buckley, Stephen J. "Utilizing Excess Capacity of Current Launch Vehicles to Lift Secondary Payloads." IEEEXplore. Naval Postgraduate School Library. Article 4526295. 1 Jan. 2009. <http://ieeexplore.ieee.org/Stamp/Stamp.jsp?tp=&arnumber=4526295&isnumber=4526225>

Coelho, Roland. Teleconference. Naval Postgraduate School, Monterey. 1 Apr. 2009.

Crook, Matthew. "NPS CubeSat Launcher." Monterey: Naval Postgraduate School, 2008.

"D-Sub Female 90°." E-mail sent to the author. Conec Gimbh. Naval Postgraduate School, 1 Apr. 2009.

"DNet # 11050: Multiple Interface Payload Subsystem Envelope Drawing." E-mail sent to the author. Design Net Engineering LLC. Naval Postgraduate School, Monterey. 26 Jan. 2009.

E-mail sent to the author. Naval Postgraduate School, Monterey. 5 Mar. 2009. <http://www.tarleton.edu/~tbarker/105/Notes_handouts/105_dimensions_ppt_notes.pdf>

Harrell, Glenn. Interview. Naval Postgraduate School, Monterey. 1 Apr. 2009.

Hicks, Christina. Conference. Naval Postgraduate School, Monterey. 1 Sep. 2008.

Hicks, Christina. "NPSCuL-Lite: NPS CubeSat Launcher-Lite." E-mail sent to the author. Naval Postgraduate School, Monterey. 1 Jan. 2009.

"High-Current Density Surface Mount Schottky Rectifier." Vishay General Semiconductor, 2008. 1 Apr. 2009. <www.vishay.com>

"High Electrical & Mechanical Noise Immunity Relay: JQ Relays." E-mail sent to the author. Matsuhita Electric Works, Ltd. 1 Apr. 2009.

Horowitz, Paul, and Winfield Hill. The Art of Electronics 2nd ed. New York: Cambridge University Press, 1989.

"India's PSLV Successfully Launches Ten Satellites." 28 April 2008. Indian Space Research Organization. 20 Jan. 2009. <www.spaceref.com/new/viewpr.html?pid=25321>

"Israel plans launch of nano-satellites as low cost alternative to GPS satellites." WorldTribune. com. East West Services, Inc. 2008. 20 Jan. 2009. <http://www.worldtribune.com/worldtribune/WTARC/2008/me_israel0750_11_27.asp>

"JS-M Relays." E-mail sent to the author. Matsuhita Electric Works, Ltd. Naval Postgraduate School, Monterey. 1 Apr. 2009.

Lan, W. "Poly Picosatellite Orbital Deployer Mk III ICD." E-mail sent to the author. California Polytechnic State University, San Luis Obispo. 2007. Naval Postgraduate School, Monterey. 1 Apr. 2009.

"LM2678 Simple Switcher High Efficiency 5A Step-Down Voltage Regulator." E-mail sent to the author. National Semiconductor Corporation, 2008. Naval Postgraduate School, Monterey. 1 Apr. 2009.

"Low-Cost Launch Service." University of Toronto Institute for Aerospace Studies Space Flight Laboratory. 2008. 20 Jan. 2009. <http://www.utiassfl.net/SpecialProjects/Launch Index.html>www.isro.org/pslv-c9/photo/PadE3a.jpg> 1 Jan 2009.

"Maxim 12-Bit +Sign Digital Temperature Sensors with Serial Interface." Maxim Integrated Products: Sunnyvale, 2005

"Maxim Dual High-Speed 1.5A MOSFET Drivers." E-mail sent to the author. Maxim Integrated Products, Inc., 2006. Naval Postgraduate School, Monterey. 1 Apr. 2009.

McInnes, Colin R. "Simple Analytic Model of the Long-Term Evolution of Nanosatellite Constellations." Journal of Guidance, Control, and Dynamics 2000. 0731-5090 vol.23 no.2 (332-338). 2000. 20 Jan. 2009. <http://www.aiaa.org.libproxy.nps.edu/content.cfm?pageid=406>

MIL-HDBK-340A: Department of Defense Handbook Test Requirements for Launch, Upper-Stage, and Space Vehicles Vol I: Baselines. Defense Standardization Program Office (DLSC-LM): Los Angeles, 1999.

"Model 9102G: Nonexplosive Release Mechanism (.250-28 Thread)." E-mail sent to the author. NEA Electronics, Inc. Naval Postgraduate School, Monterey, 1 Apr. 2009.

"Multilayer Ceramic Capacitors (For General Electronic Equipment)." E-mail sent to the author. Panasonic, 2009. Naval Postgraduate School, Monterey. 1 Apr. 2009.

Murphy, Gerald. "The Multiple Interface Payload Subsystem." E-mail sent to the author. 18 Dec. 2008.

Newman, James H., Daniel Sakoda, and Rudolph Panholzer. "CubeSat Launchers, ESPA-rings, and Education at the Naval Postgraduate School." Presentation, 21st Annual AIAA/USU Conference on Small Satellites, August 2007

"NUD3112 Integrated Relay, Inductive Load Driver." Semiconductor Components LLC, 2009. 1 Apr. 2009. <http://onsemi.com>

O'Dwyer,Gerard. "Helinski Swedish Firm Sees Future in Micro Technologies." Defense News. Gannett Co., Inc., and NewsBank, Inc. 2004. 20 Jan. 2009. <http://docs.newsbank.com.libproxy.nps.edu/openurl?ctx_ver=z39.88-2004&rft_id=info:sid/iw.newsbank.com:AFNB:DFNB&rft_val_format=info:ofi/fmt:kev:mtx:ctx&rft_dat=11892AEAE14D2198&svc_dat=InfoWeb:aggregated5&req_dat=0D0CB5FC0F5C3AD5>

"PCB Relay G5RL." Omron Electronic Components, LLC.:Schaumburg, 2008. 1 Apr. 2009. <http://www.components.omron.com>

Phelps, Ron. Interview. Naval Postgraduate School, Monterey. 1 May 2009.

Plattard, Serge. "New Era of Robotic and Human Space Exploration." 56th International Astronautical Congress of the International Astronautical Federation, the International Academy of Astronautics, and the International Institute of Space Law, Fukuoka, Japan, IAC-05-B5.6.A.07 21 Oct. 2005. 20 Jan. 2009. <http://www.espi.or.at/index.php?option=com_content&task=view&id=301&Itemid=1>

"Plug Assembly, Solder Cup, Size , 25 Posn, HD-20, Amplimited." Tyco Electronics Corporation: Harrisburg, 2000.

"Precision Thick Chip Film Resistors." E-mail sent to the author. Panasonic, 2007. Naval Postgraduate School, Monterey. 1 Apr. 2009.

"PSLV-C11 LiftOff." 1 Jan. 2009. <www.gufaratiblogger.com/uploads/PSLV C11%20LiftOff.jpg>

Rigmaiden, David. Interview. Naval Postgraduate School, Monterey. 1 Apr. 2009.

Sakoda, Daniel. Interview. Naval Postgraduate School, Monterey. 1 Jun. 2009.

Salehuddin, Adi. "Coordinate System." E-mail sent to the author. Naval Postgraduate School, Monterey. 3 Mar. 2009.

"Schottky Rectifiers." STMicroelectronics, 2002. 1 Apr. 2009. <http://www.st.com>

Shaffner, Jake A. The Electronic System Design, Analysis, Integration, and Constructionof the Cal Poly. State University CP1 CubeSat. 2002. 20 Jan. 2009.<http://polysat.calpoly.edu/PublishedPapers/JakeSchaffner_srproj.pdf>

"Socket Cap Screws." McMaster-Carr Supply Company, 2009. 1 Mar. 2009. <http://www.mcmaster.com/#socket-cap-screws/=27dme4>

"Solid Tantalum Chip Capacitors Tantamount Conformal Coated, Maximum CV, Low ESR." Vishay Sprague, 2008. 1 Apr. 2009. <www.vishay.com>

"Surrey Missions: TiungSAT-1." Surrey Satellite Technology LTD. Guilford, Surrey, 2009. 20 Jan. 2009. <http://microsat.sm.bmstu.ru/library/SSTL/Mission_TiungSAT.pdf>

"THT/SMT Power Inductors: Toroid-Designed for National's 260 kHz Simple Switcher." Pulse, 2006. 1 Apr. 2009. <www.pulseeng.com>

"Tsinghua-1." 1 Jan. 2009. <http://centaur.sstl.co.uk/SSHP/pix/Tsinghua-1.jpg>

"Twin Power Automotive Relay: CF Relays." E-mail sent to the author. Matsushita Electric Works, Ltd. 1 Apr. 2009.

Worth, Robert. E-mail sent to the author. Naval Postgraduate School, Monterey. 4 Mar. 2009.

Design Net Engineering LLC. Golden, 2009. 1 Sep. 2008. <www.design-group.com>

Xinhua News Agency. "China Develops First Nano-satellite." China.org.cn. 2004. 20 Jan. 2009. <www.china.org.cn/english/scitech/93341.htm>

Xiong, Jiangping et al. "On Board Computer Subsystem Design for the Tsinghua Nanosatellite" Beijing and Tshinghua Universities. AIAA-2002-1922. 20th AIAA International Communication Satellite Systems Conference and Exhibit, Montreal, Quebec, 15 May 2002. 20 Jan. 2009. <http://www.aiaa.org.libproxy.nps.edu/content.cfm?pageid=406>

Zhang, Haiyun et al. “The GPS Receiver For Micro/Nanosatellites.” NanoTech 2002. “At the Edge of Revolution.” AIAA-2002-5753. Houston 12 Sep 2002. American Institution of Aeronautics and Astronautics, Inc. 2009. 20 Jan. 2009. <http://www.aiaa.org/content.cfm?pageid=406&gTable=Paper&gID=5271>

THIS PAGE INTENTIONALLY LEFT BLANK

APPENDIX A

NAVAL POSTGRADUATE SCHOOL CUBESAT LAUNCHER-LITE PROTOTYPE SEQUENCER FUNCTIONAL REQUIREMENTS DOCUMENT

VERSION 2

LAST UPDATED

13 MAY 2009

Revision	Date	Author	Notes
1	03/10/2009	A. D. Harris	Initial Concept
2	05/13/2009	A.D. Harris	Design Net Inputs

1. General Information

1.1. Purpose

1.1.1. The purpose of this functional requirements document is to document the functionality and provide an in-depth understanding of the Naval Postgraduate School Cube Satellite Launcher Light Version (NPSCuL-Lite) sequencer. Furthermore, this document will provide: the scope, references, notes, points of contact, background information, objectives, procedures, equipment being used, inputs and outputs, provisions in design, deficiencies, improvements, impacts, assumptions and constraints, detailed characteristics, failure contingencies, design considerations, system description, system functions, flexibility, and the environment.

1.1.2. The NPSCuL-Lite sequencer is a functional simulator for the Multiple Interface Payload Subsystem (MIPS) created by Design Net Engineering, LLC. The school's device will not be flown in to space. Rather, it will be designed for educational purposes, for additional information and support to the NPSCuL-Lite team, and for future work that may deal with creating a flight article. The design of the sequencer will resemble Design Net's MIPS with additional limited capabilities.

1.1.3. The NPSCuL-Lite sequencer is a product that assembles the appropriate resources in a common structure to support a specific mission. This product may include a telemetry multiplexer that can collect, collate, format and transmit payload data. Finally, it controls deployment of between 8 to 10 auxiliary payloads according to a pre-programmed sequence.

1.1.4. The sequencer design should be able to accommodate a variety of deployment devices. Deployments must be programmable from mission to mission without hardware modifications. Ease of configuration and programmability will enable rapid integration and maximum flexibility.

1.2. Scope

1.2.1. The scope of this document includes the contents of the sequencer and excerpts from other systems that the sequencer will be interfacing with. The primary mission of this document is to delineate the functionality of the sequencer. This document captures interface requirements, derived requirements, and functional requirements specifications for the sequencer that will be a functional simulator of a device that supports rideshare payload deployment on the Falcon, Minotaur and EELV launch vehicles. In regard to the device, the document will only cover material that goes as far as what would be considered for the NPSCuL-Lite project. This is the sole source of all top level functional requirements specifications for the NPSCuL-Lite sequencer that will flow down to individual requirements specifications for the boards that build up the component.

1.2.2. Since NPSCuL-Lite sequencer is a device that simulates Design Net's MIPS, it may have some potential applications for the boards to operate in a GTO orbit as well as LEO. In the event that the functional simulator becomes space qualified, it will only be operated for short-lived situations (less than 24 hours).

1.3. Project References

1.3.1. NPSCuL documents

1.3.2. NPS SSAG faculty

1.3.3. www.design-group.com

1.3.4. www.parallax.com

1.3.5. www.digikey.com

1.3.6. Multiple Interface Payload Subsystem (MIPS) Product Specification: DNet_11036

1.3.7. Deployment Subsystem Electronics (DSE) Requirements Specification: DNet Document_11030

1.4. Acronyms and Abbreviations

1.4.1. ABC – The common carrier capability on the aft end of the Atlas Centaur Upper Stage designed with a standard 15” (lightband type) mechanical interface.

1.4.2. BIST – built in system test

1.4.3. BS(#) – Basic Stamp Module Version Number (#)

1.4.4. Cal Poly – California Polytechnic University San Luis Obispo

1.4.5. CG – Center of Gravity

1.4.6. COTS – Commercially Available off the Shelf

1.4.7. CubeSat – Cube Satellite

1.4.8. DSE – Deployment Subsystem Electronics

1.4.9. ESD – Electrostatic Discharge

1.4.10. EMI – Electromagnetic Interference

1.4.11. I-DEAS – CAD software used to develop models

1.4.12. LEO - Low Earth orbit

1.4.13. LV – Launch Vehicle

1.4.14. MIPS – Multiple Interface Payload Subsystem

1.4.15. MLB – Motorized Lightband is the mechanism of r separating and staging of the primary payload, and nanosat or FalconSAT-class of secondary payloads.

1.4.16. NPS – Naval Postgraduate School

1.4.17. NRO – Naval Reconnaissance Office

1.4.18. NX-6 – CAD software used to develop models

1.4.19. PBASIC – Program used by the basic Stamp microcontrollers

1.4.20. P-POD – Poly Picosatellite Orbital Deployer is the housing and deployment mechanism for the CubeSat-class of secondary payloads.

1.4.21. RSA – Rideshare adapter is a secondary payload carrier structure, which includes all the harnesses and flight boxes (e.g. MIPS).

1.4.22. SPS – Secondary Payload Subsystem consists of the RSA and all secondary payloads that are mounted to it.

1.4.23. TBD – To be determined

1.4.24. ULA – United Launch Alliance

1.5. Language

Throughout the document, the following verbs will have the meaning specified below:

"Shall" – the use of this word expresses a mandatory requirement, which must be carried forward in lower level specifications. A "shall" statement describes a testable feature of the system.

"Should" – This expresses a preference.

"Must" – This statement describes a testable feature of the system.

"Will" – Expresses an intended service. This describes a system feature.

"May or Can" – This expresses a permissible practice

1.6. Points of Contact

1.6.1. Information

1.6.1.1. Tony Harris

1.6.1.2. Justin Jordan

1.6.1.3. Christina Hicks

1.6.1.4. James Newman

1.6.1.5. Daniel Sakoda

1.6.1.6. David Rigmaiden

1.6.1.7. Roland Coelho (Cal Poly)

1.6.2. Coordination

1.6.2.1. Design-Net Engineering for the real sequencer

1.6.2.2. ULA for envelope constraints

1.6.2.3. NRO for funding

1.6.2.4. Cal Poly for P-POD integration

1.6.2.5. STP

2. Current System Summary

2.1. Background

Currently, there is no funding for a sequencer to be procured for the NPSCuL-Lite project. The sequencer that NPS is creating is a backup model in case the NPSCuL team does not have the funding to buy a commercial sequencer. The sequencer is a box that contains electrical and logical components to perform specific functions. The NPSCuL-Lite sequencer is a device to open 8 P-PODs individually in a certain time interval.

2.2. System Objectives and Current Functionality

2.2.1. Imitate the Design-Net model

2.2.2. House the circuitry and logic for the P-POD opening mechanism

2.2.3. Timed opening sequence for the 8 P-PODs

2.2.4. Open 8 P-PODs, one at a time, every 2 seconds

2.2.5. Provide proper reliability through redundancy

2.3. Current Methods and Procedures

Electrical circuits will be created on circuit boards using standard electrician methods. A program will be written for the Stamp microcontroller to control the logical commands of the circuit. This program while interfaced with the rest of the electrical components will be tested for proper function. Once an appropriate amount of testing has been completed the circuit will be re-created for further design analysis.

2.3.1. Equipment Being Used

2.3.1.1. (1) Soldering iron to solder electrical joints together

2.3.1.2. (1) Breadboard for initial circuitry creation

2.3.1.3. (3) Cards for sequencer board development

2.3.1.4. (3) IC reg simple switcher

2.3.1.5. (3) Inductor

2.3.1.6. (3) Capacitor Tant LOESR 100 µF

2.3.1.7. (3) Diode Schottky

2.3.1.8. (6) Transistor NPN to act as switches and provide 5V power supply

2.3.1.9. (6) 28V power supplies to power the unit

2.3.1.10. (9) Capacitor Tant 15 µF

2.3.1.11. (3) Parallax Stamp microcontroller to store and run the commands necessary for P-POD opening

2.3.1.12. (3) Voltage Regulators to step down 28V voltages to 5-12V voltages

2.3.1.13. (24) IC inductive load drivers to actuate the relays for the circuit

2.3.1.14. (24) IC mosfet driver dual noninverting

2.3.1.15. (24) Relay GP SPST-NO

2.3.1.16. (24) Relay PWR HI-CAP 200MW 12VDC PCB

2.3.1.17. (24) Relay PWR SPST 16A 12VDC PCB

2.3.1.18. (24) Relay Auto 10A 12VDC sealed PCB

2.3.1.19. (24) IC MUX/DEMUX analog HS 24-SOIC

2.3.2. Input and Output

2.3.2.1. The Input and Output section TBD

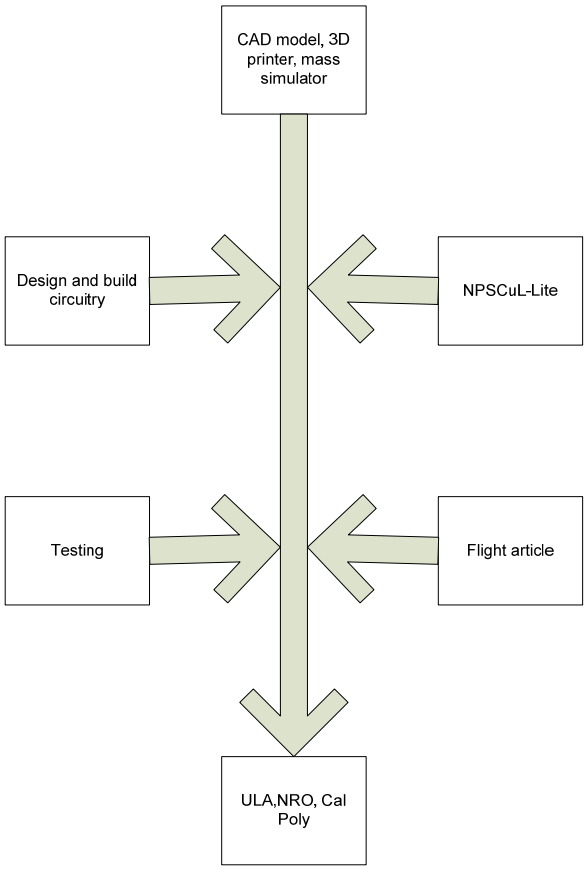
2.3.3. Provisions in the Existing System Design

2.3.3.1. Provisions TBD

2.3.4. Deficiencies

2.3.4.1. Deficiencies TBD

3. Proposed Methods and Procedures



Requirements Flowdown

The NPSCuL-Lite sequencer is a modular embedded controller. The circuit boards function as a deployer to open 8 P-PODs individually in a certain time interval. These P-PODs are produced by an integrated effort between NPS and Cal Poly. The NPSCuL-Lite structure will be holding 8 3U P-PODs that will store and launch CubeSat.

3.1. Summary of Improvements

3.1.1. Proposed Requirements

3.1.1.1. The sequencer board is designed to be easily configurable and a stand-alone entity.

3.1.1.2. The sequencer box will be mounted externally on the NPSCuL-Lite structure.

3.1.1.3. It will have a readily accessible port to re-program software before sent to orbit.

3.1.1.4. Redundancy is built in the system by having duplicate components and wiring in the event of a failure. The circuitry is set up so that if the redundancy methods fail, and one P-POD will not open, this failure does not affect the rest of the P-POD openings.

3.1.1.5. The sequencer box will be launched in the "off" condition so the high RF fields associated with range will not need to be accounted for in shielding.

3.1.1.6. Sequencer will have a software configurable embedded controller

3.1.1.7. The NPSCuL-Lite sequencer's design is based off the of the DSE board created by Design-Net Engineering.

3.1.2. Functional Improvements

3.1.2.1.The NPSCuL-Lite Sequencer will provide extra wiring and duplicate components to perform the same functions for mission success. For example, if the circuitry and redundant components for P-POD #1 fail, and P-POD #1 door does not open, this will not affect P-POD doors #2 to #8.

3.1.3. Improvements to Existing Capabilities

3.1.3.1. The NPSCuL-Lite Sequencer will provide redundancy to mitigate losses in the event of failure. The DSE model does provide redundancy for its components.

3.1.4. Timeliness

3.1.4.1. No added improvement in timeliness exists thus far.

3.2. Summary of Impacts

Currently, there are no out of the ordinary anticipated impacts on the existing development of the system, organizational and operational environments of the user.

3.2.1. User Organizational Impacts

3.2.1.1. Several people will be primarily responsible for the production of the NPSCuL-Lite sequencer. At a minimum, the principal investigator, engineering faculty members, a thesis student responsible for the design, creation, and interfacing of the NPSCuL-Lite sequencer, and an assistant student to help design the electrical interface of the sequencer.

3.2.1.2. Various SSAG faculty members will be adjunct sources of mentoring and guidance in the project.

3.2.1.3. The education/knowledge level of the students working on this project is one student working on a baccalaureate in a technical degree, and another student working on a master's technical degree. For further detailed knowledge, expert engineers in the program will be notified.

3.2.1.4. Training and use of the basic Stamp software to create the program. Background in electrical work to create the circuitry for the sequencer.

3.2.2. User Operational Impacts

3.2.2.1. Currently, there are no operational impacts to the organization during the use of the proposed system.

3.2.3. User Developmental Impacts

3.2.3.1. The student responsible for the creation of the sequencer shall give all the effort necessary to produce a prototype model within the timeframe of his academic lifetime.

3.3. Assumptions and Constraints

3.3.1. NRO funding may not come through for the procurement of a COTS sequencer.

3.3.2. The prototype has limited funds, manpower, and other resources. It will have very limited functionality compared to the DSE. For example, it will not have the depth of capability to shield radiation. If exposed to a radiation intensive environment, there is no assurance that the sequencer will be able to complete the mission.

4. Detailed Characteristics

4.1. Specific Performance Requirements

4.1.1. Accuracy and Validity

4.1.1.1. The CG allowance that ULA provides gives the NPSCuL-Lite structure and sequencer 0.5 in from the origin of the (+) Y axis.

4.1.1.2. The Sequencer's mass properties put the NPSCuL-Lite out of the CG specification from the ULA CG allowance. The CG in the X and the Z planes are within tolerance. However, the CG in the Y plane is 0.27 inches outside of the acceptable ULA tolerance.

NPSCuL Lite Mass Properties						
				Center of Gravity		
Component	Volume (cubic inches)	Mass (lbs)	Mass (kg)	x	y	z
Adapter	33.42	3.38	1.53	0.00	0.00	1.02
Base Plate	104.86	10.59	4.80	0.00	0.00	2.35
Sidewall 1	59.21	5.98	2.71	9.12	-0.11	8.60
Sidewall 2	59.21	5.98	2.71	0.11	-9.13	8.60
Sidewall 3	59.21	5.98	2.71	-9.12	0.11	8.60
Sidewall 4	59.21	5.98	2.71	-0.11	9.12	8.60
Bracket 1	6.59	0.67	0.30	9.01	9.01	8.60
Bracket 2	6.59	0.67	0.30	9.01	-9.01	8.60
Bracket 3	6.59	0.67	0.30	-9.01	-9.01	8.60
Bracket 4	6.59	0.67	0.30	-9.01	9.01	8.60
Sequencer	103.01	10.10	4.58	0.00	10.92	6.78
P-POD 1		4.95	2.25	6.14	6.44	12.90
P-POD 2		4.95	2.25	6.14	1.21	12.90
P-POD 3		4.95	2.25	6.44	-6.14	12.90
P-POD 4		4.95	2.25	1.12	-6.14	12.90
P-POD 5		4.95	2.25	-6.14	-6.44	12.90
P-POD 6		4.95	2.25	-6.14	-1.21	12.90
P-POD 7		4.95	2.25	-6.44	6.14	12.90
P-POD 8		4.95	2.25	-1.12	6.14	12.90
3U CubeSat 1		6.60	3.00	6.25	6.44	10.99
3U CubeSat 2		6.60	3.00	6.25	1.21	10.99
3U CubeSat 3		6.60	3.00	6.44	-6.25	10.99
3U CubeSat 4		6.60	3.00	1.21	-6.25	10.99
3U CubeSat 5		6.60	3.00	-6.25	-6.44	10.99
3U CubeSat 6		6.60	3.00	-6.25	-1.21	10.99
3U CubeSat 7		6.60	3.00	-6.44	6.25	10.99
3U CubeSat 8		6.60	3.00	-1.21	6.25	10.99
Total		143.05	64.88	0.00	0.77	9.90

NPSCuL-Lite Sequencer CG Mass and CG Characteristic (From Crook)

4.1.2. Power

The power distribution will be derived by a battery source that will be integrated in the sequencer unit.

4.1.2.1. The sequencer shall be designed to operate off of standard voltages (+28V)

4.1.2.2. Power input to any configuration of the sequencer chassis shall be 28V nominal LV power or 28V nominal umbilical power (assuming the LV and umbilical power come via two separate connectors).

4.1.2.3. All boards shall provide the necessary regulated secondary voltages and power sequencing for on-board functions

4.1.2.4. The design shall ensure that while the sequencer is powered by the umbilical that it will not accidently open the P-PODs.

4.1.2.5. Pins on the Stamp controller that will receive input voltage TBD

4.1.2.6. The sequencer board and the chassis shall launch in an un-powered or cold state

4.1.2.7. Provisions will be made on the power input connector to accept power from the battery source or the LV power interface.

4.1.2.8. Power on RESET (POR) circuitry shall return all circuits on the sequencer to a “safe” mode upon abnormal conditions.

4.1.2.9. POR shall not affect the ability of the sequencer to complete its mission

4.1.2.10. Over-current protection shall be implemented on all outputs

4.1.2.11. The system will be launched in an un-powered state

4.1.2.12. Each channel should be able to respond to command from the launch vehicle through RS422/485 (TBD).

4.1.2.13. The Sequencer will be properly grounded per the EMI requirements.

4.1.2.14. A crow bar circuit will be implemented to protect internal circuitry

4.1.3. Housekeeping

4.1.3.1. Each board in the chassis is required to provide its own housekeeping. It is intended for basic board level status.

4.1.3.2. The HK data shall be used as a part of BIST

4.1.4. Other Electrical Functions

4.1.4.1. All boards except the power converter shall implement an RS-422 serial port interface to an external connector

4.1.4.2. The minimum speed of the serial connection shall be 1200 baud and the maximum speed shall be 19200 baud. The speed shall be software configurable

4.1.4.3. Each board shall have a software configurable embedded controller

4.1.4.4. Each board shall provide BIST capability with visual indication/feedback to verify that the board is ready for operation.

4.1.5. Separation Sense

4.1.5.1. Each P-POD includes primary and redundant sensors which are switches wired to either close or open on successful deployment. Each sensor shall have an associated separation sense channel/circuit

4.1.5.2. The sequencer will provide 2A current to each primary and redundant circuits going to the NEA 9102G

4.1.5.3. The NEA will open at 100 to 120 msec with 2A of current

4.1.5.4. Telemetry from the P-POD opening shall be sent back to the Stamp controller

4.1.6. NEA Requirements

4.1.6.1. The sequencer will provide 2A current to each primary and redundant circuits going to the NEA 9102G

4.1.6.2. The NEA will open at 100 to 120 msec with 2A of current

4.1.7. Timing

4.1.7.1. 2 seconds should lapse between each “Open P-POD” command issued from the sequencer

4.1.7.2. Other timing limits TBD

4.1.8. Capacity Limits

4.1.8.1. The sequencer shall not consume a maximum of 5W when fully operational

4.1.8.2. The sequencer will provide 8 high current switch circuits for 8 channels rated at 28V, 6A

4.1.8.3. the sequencer shall support a maximum of 8 deployment channels as a single output per payload

4.1.8.4. The sequencer shall also support 8 redundant deployment channels

4.1.8.5. Each channel shall have its own output connector

4.1.8.6. Connectors and pin-outs for all 8 channels shall be identical and the pin-out must be specified in proprietary documentation

4.1.8.7. The circuitry leading to the P-POD, excluding the Stamp controller and associated components will have tolerances of at least 5-7A and Voltage ranges between 28 +/- 6V.

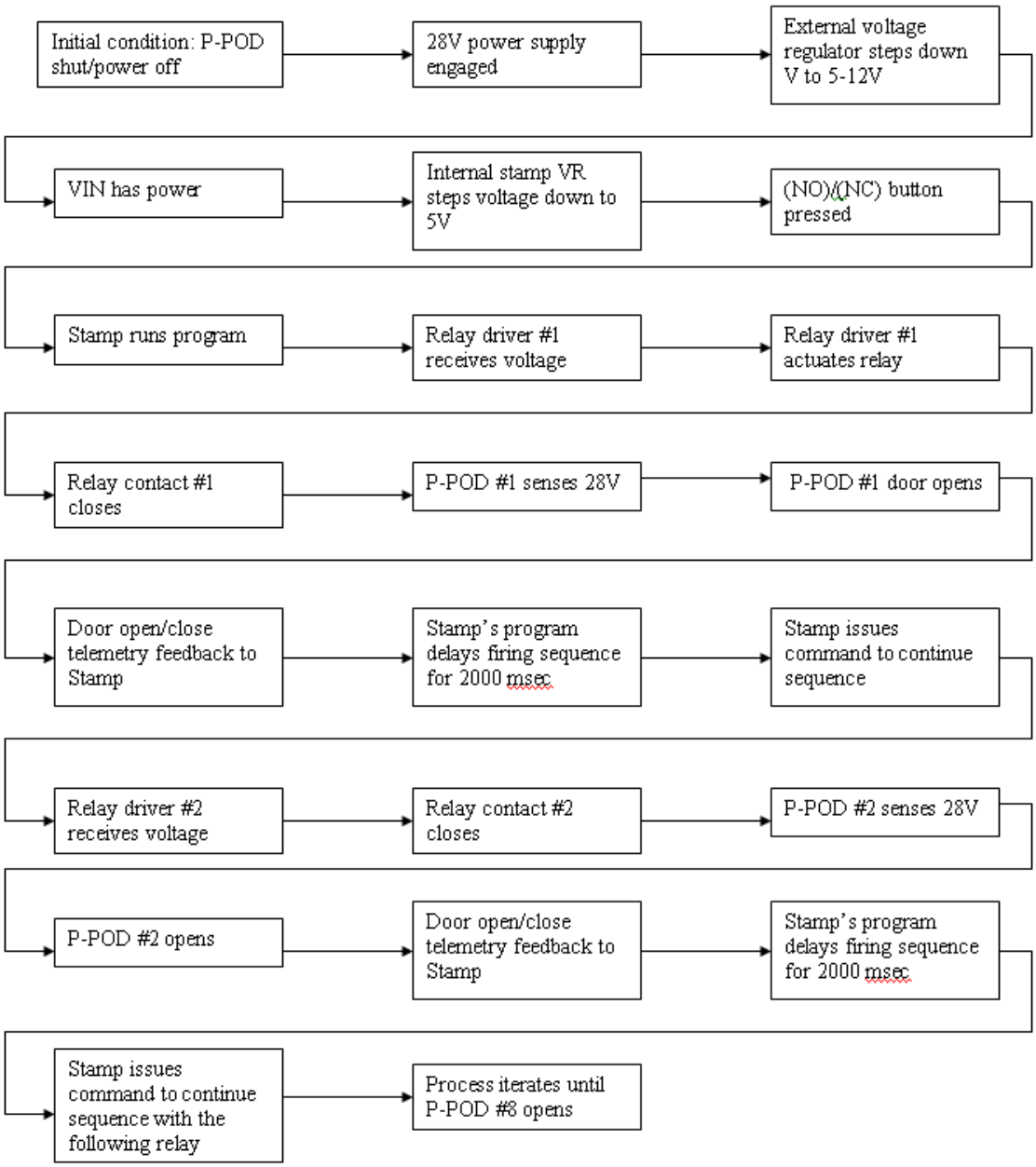
4.1.8.8. Any values outside the voltage and current tolerances will be considered as an anomaly.

4.1.9. Capability Elimination

4.1.9.1. As it stands, the NPSCuL-Lite sequencer does not coordinate with other boards. This is due to the fact that the NPSCuL-Lite design is simple and does not require various boards to perform distinct functions. Simply, the project's design is to open P-PODs at a certain acceptable rate that allows CubeSats to be deployed successfully in the LEO environment.

4.1.9.2. The NPSCuL-Lite sequencer software will have re-configurability all the way up to launch. However, there will be no re-configurability on orbit. Also, at this stage of development, the controller is not radiation tolerant for the LEO environment. Therefore software anomalies may occur.

4.2. Functional Area System Functions



System Flow Model

4.3. Input and Output

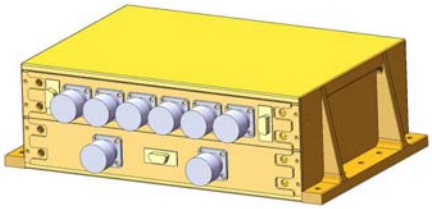
4.3.1. Green light indicating power is received by the sequencer. Telemetry should be sent back to the Stamp controller (doors opening).

4.4. Failure Contingencies

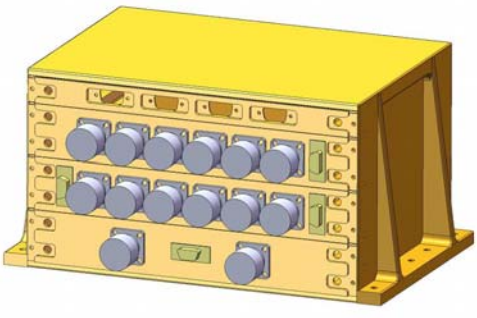
4.4.1. Operational failure methods TBD

5. Design Considerations

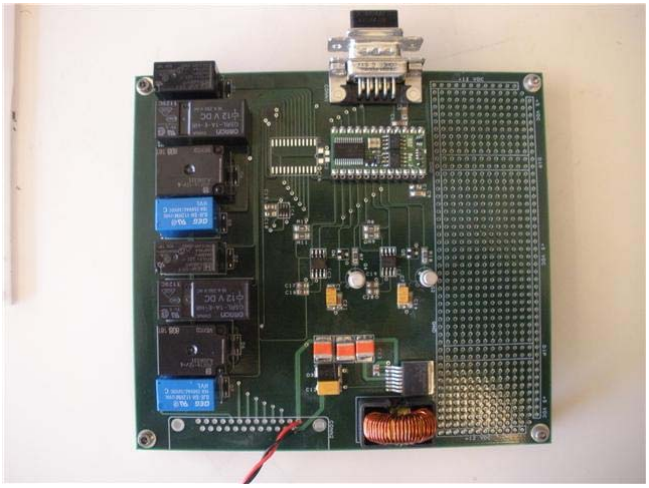
5.1. System Description



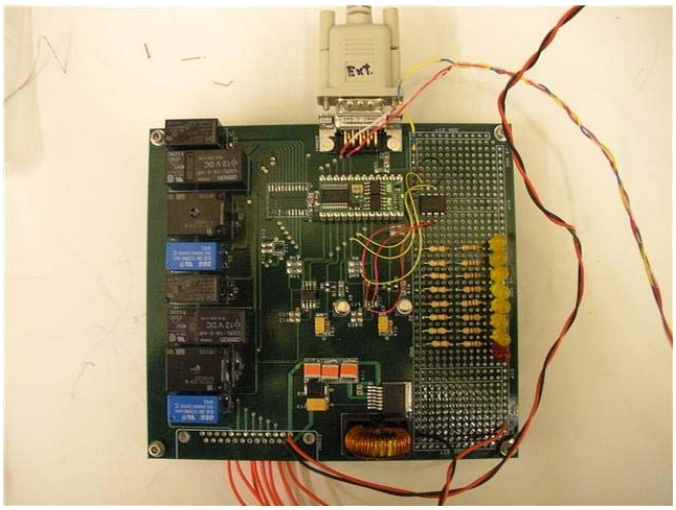
MIPS 4” Height Configuration (From Murphy)



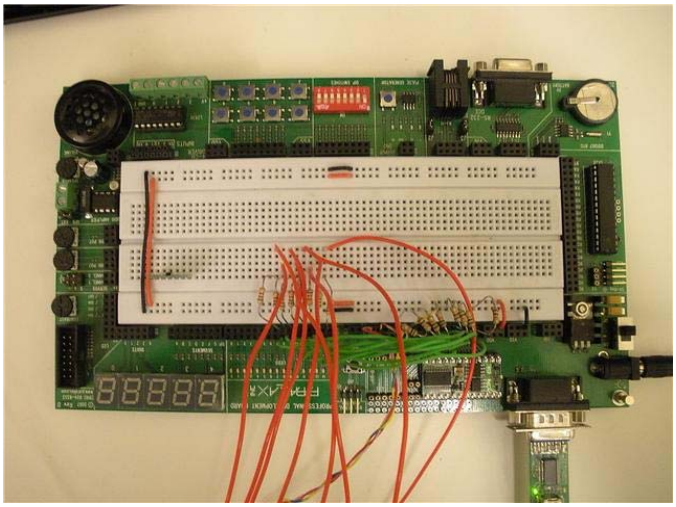
MIPS 7” Height Configuration (From Murphy)



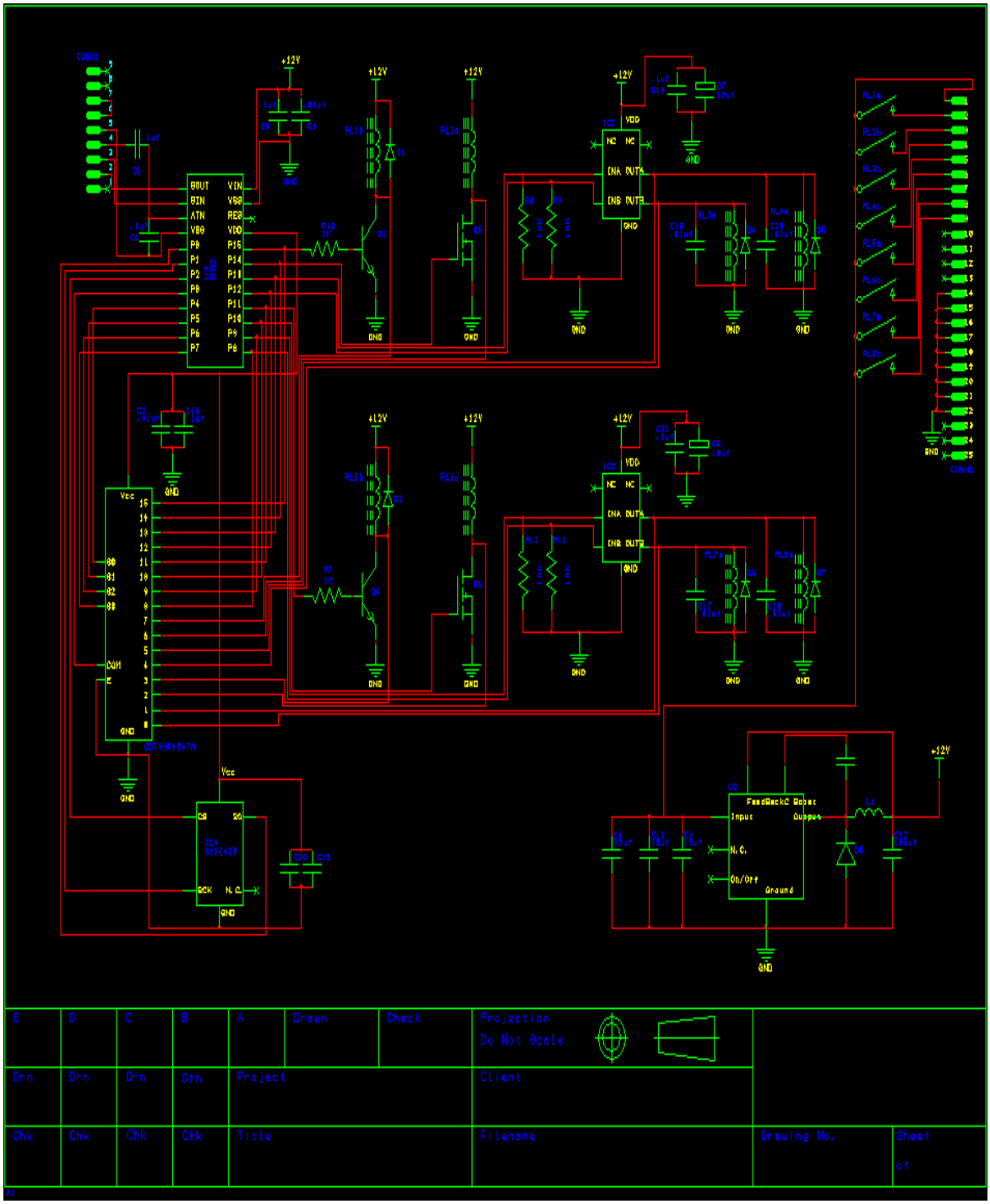
Primary Test Board



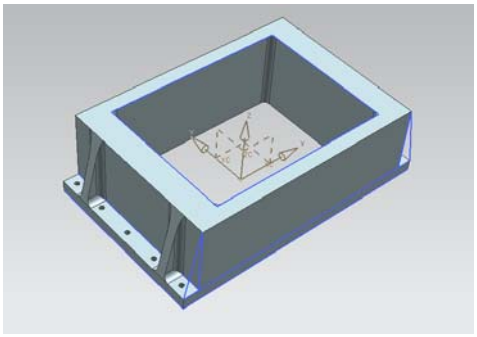
Redundant Test Board



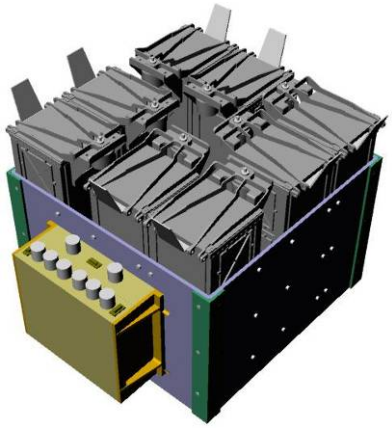
Communication Board



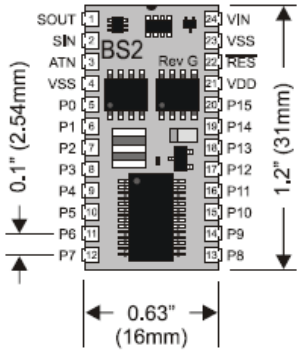
Stamp and P-POD Circuitry Conceptual Design



Sequencer Mass Model Simulator (For NPSCuL-Lite Vibration Testing)



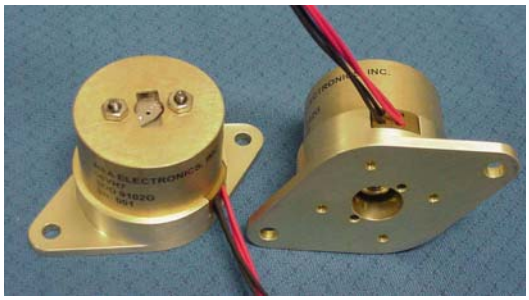
NPSCuL-Lite and Sequencer Mounted Externally (From Crook)



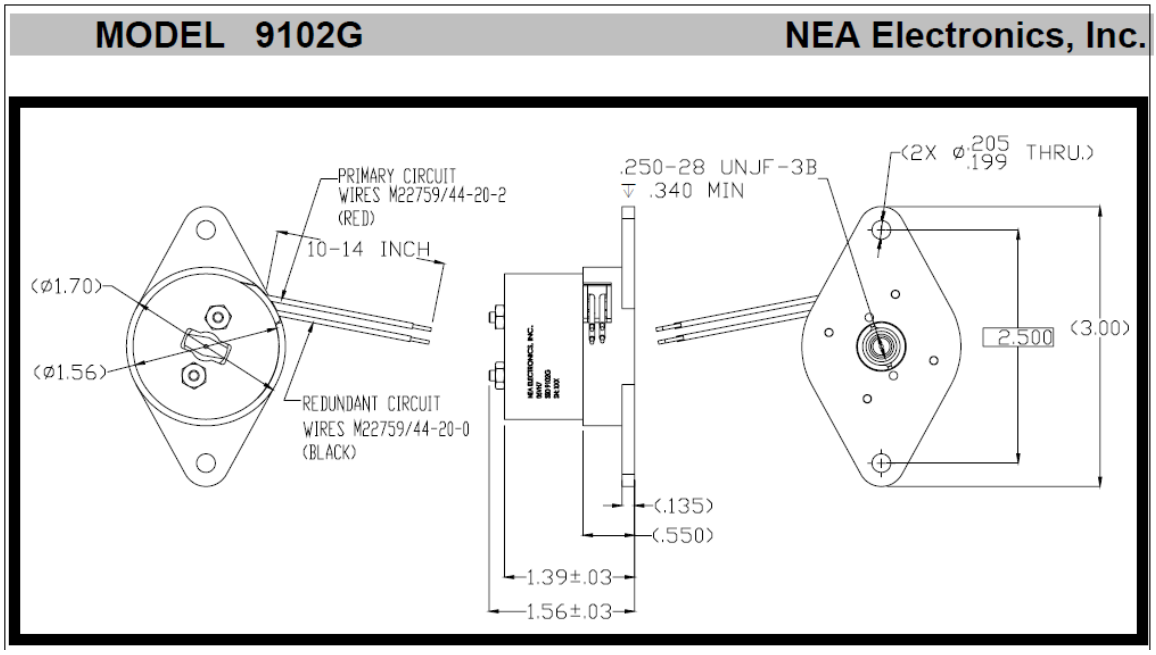
Basic Stamp 2 (From Basic Stamp Syntax and Reference Manual Version 2.2)

Pin	Name	Description
1	SOUT	Serial Out: connects to PC serial port RX pin (DB9 pin 2 / DB25 pin 3) for programming.
2	SIN	Serial In: connects to PC serial port TX pin (DB9 pin 3 / DB25 pin 2) for programming.
3	ATN	Attention: connects to PC serial port DTR pin (DB9 pin 4 / DB25 pin 20) for programming.
4	VSS	System ground: (same as pin 23) connects to PC serial port GND pin (DB9 pin 5 / DB25 pin 7) for programming.
5-20	P0-P15	General-purpose I/O pins: each can sink 25 mA and source 20 mA. However, the total of all pins should not exceed 50 mA (sink) and 40 mA (source) if using the internal 5-volt regulator. The total per 8-pin groups (P0 – P7 or P8 – 15) should not exceed 50 mA (sink) and 40 mA (source) if using an external 5-volt regulator.
21	VDD	5-volt DC input/output: if an unregulated voltage is applied to the VIN pin, then this pin will output 5 volts. If no voltage is applied to the VIN pin, then a regulated voltage between 4.5V and 5.5V should be applied to this pin.
22	RES	Reset input/output: goes low when power supply is less than approximately 4.2 volts, causing the BASIC Stamp to reset. Can be driven low to force a reset. This pin is internally pulled high and may be left disconnected if not needed. Do not drive high.
23	VSS	System ground: (same as pin 4) connects to power supply's ground (GND) terminal.
24	VIN	Unregulated power in: accepts 5.5 - 15 VDC (6-40 VDC on BS2-IC Rev. e, f, and g), which is then internally regulated to 5 volts. Must be left unconnected if 5 volts is applied to the VDD (+5V) pin.

Basic Stamp 2 Pin Descriptions (From Basic Stamp Syntax and Reference Manual Version 2.2)



NEA (From Model 9102G: Nonexplosive Release Mechanism (.250-28 Thread))



NEA Mechanical Interface (From Model 9102G: Nonexplosive Release Mechanism (.250-28 Thread))

5.2. System Functions

5.3. Flexibility

6. Environment

6.1. Equipment Environment

6.1.1. The sequencer shall be tested in accordance with the appropriate qualification testing approach.

6.2. Software Environment

6.2.1. PBASIC language will be used as the programming language for the microcontroller

6.2.2. The BS2 is the model of the basic Stamp that will be used for the processing of logic

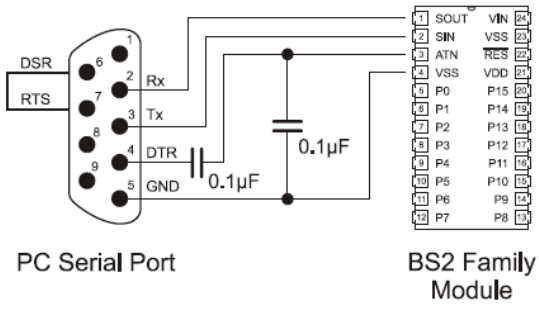
Products	BS1	BS2	BS2e
Environment	0° - 70° C (32° - 158° F) **	0° - 70° C (32° - 158° F) **	0° - 70° C (32° - 158° F) **
Microcontroller	Microchip PIC16C56a	Microchip PIC16C57c	Ubicom SX28AC
Processor Speed	4 MHz	20 MHz	20 MHz
Program Execution Speed	~2,000 instructions/sec.	~4,000 instructions/sec	~4,000 instructions/sec
RAM Size	16 Bytes (2 I/O, 14 Variable)	32 Bytes (6 I/O, 26 Variable)	32 Bytes (6 I/O, 26 Variable)
Scratch PadRam	N/A	N/A	64 Bytes
EEPROM (Program) Size	256 Bytes, ~80 instructions	2K Bytes, ~500 instructions	8 x 2K Bytes, ~4,000 inst
Number of I/O Pins	8	16 + 2 Dedicated Serial	16 + 2 Dedicated Serial
Voltage Requirements	5 - 15 vdc	5 - 15 vdc	5 - 12 vdc
Current Draw@ 5 volts	1 mA Run, 25 µA Sleep	3 mA Run, 50 µA Sleep	25 mA Run, 200 µA Sleep
Source/Sink Current per I/O	20 mA / 25 mA	20 mA / 25 mA	30 mA / 30 mA
Source/Sink Current per unit	40 mA / 50 mA	40 mA / 50 mA per 8 I/O pins	60 mA / 60 mA per 8 I/O pins
PBASIC Commands*	32	42	45
PC Interface	Serial (w/BS1 Serial Adapter)	Serial (9600 baud)	Serial (9600 baud)
Windows Text Editor Version	Stampw.exe (v2.1 and up)	Stampw.exe (v1.04 and up)	Stampw.exe (v1.096 and up)

Basic Stamp Requirements (From Basic Stamp Syntax and Reference Manual Version 2.2)

6.2.3. If necessary, the NPSCuL-Lite team will procure industrial-rated version of the basic Stamp models which have an environmental tolerance range of -40°C to +85°C.

6.3. Communications Requirements (Section TBD)

6.3.1. Communications Overview



BS2 Connection to RS-422 (From Basic Stamp Syntax and Reference Manual Version 2.2)

6.3.2. Communications Hardware

6.3.3. Communications Software

6.4. Thermal Requirements for the LEO Environment

6.4.1. The board components shall be designed to operate in orbit over the temperature range of -25^{o}C to + 55^{o}C.

6.4.2. The board electronics shall be tested over the temperature range of -35^{o}C to + 65^{o}C.

6.5. Interfaces

6.5.1. Interfaces section TBD

6.6. Summary of Impacts (Section TBD)

6.6.1. IS Organizational Impacts

6.6.2. IS Operational Impacts

6.6.3. IS Developmental Impacts

6.7. Failure Contingencies (Section TBD)

6.7.1. Restart/Recovery

6.7.2. Other Contingencies

6.7.3. Assumptions and Constraints

WORKS CITED

Basic Stamp Syntax and Reference Manual Version 2.2. Parallax Inc., 2005. 1 Jul. 2008. <http://www.parallax.com>

"DNet # 11050: Multiple Interface Payload Subsystem Envelope Drawing." E-mail sent to the author. Design Net Engineering LLC. Naval Postgraduate School, Monterey. 26 Jan. 2009.

Coelho, Roland. Teleconference. Naval Postgraduate School, Monterey. 1 Apr. 2009.

Crook, Matthew. "NPS CubeSat Launcher." Monterey: Naval Postgraduate School, 2008.

"Model 9102G: Nonexplosive Release Mechanism (.250-28 Thread)." E-mail sent to the author. NEA Electronics, Inc. Naval Postgraduate School, Monterey, 1 Apr. 2009.

Murphy, Gerald. "The Multiple Interface Payload Subsystem." E-mail sent to the author. 18 Dec. 2008.

"2N2219/22A High Speed Switches." E-mail sent to the author. STMicroelectronics, 2003. Naval Postgraduate School, Monterey. 1 Apr. 2009.

"D-Sub Female 90^{o}." E-mail sent to the author. Conec Gimbh. Naval Postgraduate School, 1 Apr. 2009.

"High-Current Density Surface Mount Schottky Rectifier." Vishay General Semiconductor, 2008. 1 Apr. 2009. <www.vishay.com>

"High Electrical & Mechanical Noise Immunity Relay: JQ Relays." E-mail sent to the author. Matsuhita Electric Works, Ltd. 1 Apr. 2009.

"JS-M Relays." E-mail sent to the author. Matsuhita Electric Works, Ltd. Naval Postgraduate School, Monterey. 1 Apr. 2009.

Lan, W. "Poly Picosatellite Orbital Deployer Mk III ICD." E-mail sent to the author. California Polytechnic State University, San Luis Obispo. 2007. Naval Postgraduate School, Monterey. 1 Apr. 2009.

"LM2678 Simple Switcher High Efficiency 5A Step-Down Voltage Regulator." E-mail sent to the author. National Semiconductor Corporation, 2008. Naval Postgraduate School, Monterey. 1 Apr. 2009.

"Maxim 12-Bit +Sign Digital Temperature Sensors with Serial Interface." Maxim Integrated Products: Sunnyvale, 2005

"Maxim Dual High-Speed 1.5A MOSFET Drivers." E-mail sent to the author. Maxim Integrated Products, Inc., 2006. Naval Postgraduate School, Monterey. 1 Apr. 2009.

"Multilayer Ceramic Capacitors (For General Electronic Equipment)." E-mail sent to the author. Panasonic, 2009. Naval Postgraduate School, Monterey. 1 Apr. 2009.

"NUD3112 Integrated Relay, Inductive Load Driver." Semiconductor Components LLC, 2009. 1 Apr. 2009. <http://onsemi.com>

"PCB Relay G5RL." Omron Electronic Components, LLC.:Schaumburg, 2008. 1 Apr. 2009. <http://www.components.omron.com>

"Plug Assembly, Solder Cup, Size , 25 Posn, HD-20, Amplimited." Tyco Electronics Corporation: Harrisburg, 2000.

"Precision Thick Chip Film Resistors." E-mail sent to the author. Panasonic, 2007. Naval Postgraduate School, Monterey. 1 Apr. 2009.

"Schottky Rectifiers." STMicroelectronics, 2002. 1 Apr. 2009. <http://www.st.com>

"Solid Tantalum Chip Capacitors Tantamount Conformal Coated, Maximum CV, Low ESR." Vishay Sprague, 2008. 1 Apr. 2009. <www.vishay.com>

"THT/SMT Power Inductors: Toroid-Designed for National's 260 kHz Simple Switcher." Pulse, 2006. 1 Apr. 2009. <www.pulseeng.com>

"Twin Power Automotive Relay: CF Relays." E-mail sent to the author. Matsushita Electric Works, Ltd. 1 Apr. 2009.

THIS PAGE INTENTIONALLY LEFT BLANK

APPENDIX B

NAVAL POSTGRADUATE SCHOOL CUBESAT LAUNCHER-LITE PROTOTYPE SEQUENCER ELECTRICAL BOARD UNIT THERMAL ACCEPTANCE TEST DOCUMENT

VERSION 4

LAST UPDATED

07 JUNE 2009

Revision	Date	Author	Notes
1	05/15/2009	A. D. Harris	Initial Concept
2	05/18/2009	A. D. Harris	Shortening Cycles
3	05/26/2009	A. D. Harris	Empirical Procedure
4	06/07/2009	A.D. Harris	Final Changes

1 Thermal Cycle Test Electrical and Electronic Unit Acceptance

1.1 Purpose

This section will specify the underlying reasons behind this test and the creation of the document.

1.1.1 The purpose of this test is for proof-of-concept of the electrical interface thermal requirements of the Naval Post Graduate School Cube Satellite Launcher-Lite (NPSCuL-Lite) Prototype Sequencer.

1.1.2 Furthermore, the purpose is to test performance verification of the electrical components on the test board. To do this, the tester will test the appropriate operational requirements of the device.

1.1.3 The test will detect material and workmanship defects of the unit. This will be done by thermal cycling at prescribed rates in a vacuum.

1.1.4 This test will provide the proper data, documentation, procedures, analysis, and conclusions that are needed for future student work in related areas.

1.2 Scope of this document

This section shall illuminate the extent to which the test will be performed.

1.21 This document contains the amplifying instructions for testing of the NPS CubeSat Launcher (NPSCuL-Lite) Prototype Sequencer and should accompany the NPS CubeSat Launcher-Lite Prototype Testing Procedure during testing.

1.22 Only the NPSCuL-Lite Testing Procedure and appendices must be retained after assembly.

1.23 This shall not be a full thermal acceptance test for the sequencer electrical board. Rather, this test will be a simplified version of the MIL-HDBK-340A standard.

1.24 This test shall implement some of the requirements based on the MIL-HDBK-340A standard of thermal acceptance testing.

1.25 This test shall be performed as far as necessary for the examiner's thesis requirements.

1.3 Acronyms/Definitions

1.3.1 Ambient Environment: Normal room conditions with temperatures of 23 $^{+}$/- 10°C (73 $^{+}$/- 18°F), atmospheric pressure of 101 + 2/-23 kilopascals (29.9 + 0.6/-6.8 in. Hg), and relative humidity of 50 $^{+}$/- 30%[1].

1.3.2 COTS: Commercial off the shelf products. These products are considered to be massed produced for the general consumer and will not necessarily adhere to space qualification standards.

1.3.3 Cycle: For the purposes of this test, a cycle will contain at least one hot soaking period, three transition phases, two temperature stabilization phase, and one cold soaking period.

1.3.4 LED: Light emitting Diode. This is a device that emits a light when it receives the proper signal.

1.3.5 Junction Temperature: The junction temperature refers to the temperature of the silicon die within the package of the device when the device is powered. The junction temperature can also be referred to as the operating temperature[2].

1.3.6 NPS: Naval Post Graduate School

1.3.7 NPSCuL-Lite: Naval Post Graduate School Cube Satellite Launcher-Lite. This is an innovative structure that makes efficient use of excess capacity on certain launch vehicles by carrying secondary payloads into space.

1.3.8 P-POD: Poly-Picosatellite Orbital Deployer. This is an innovative device that houses and deploys cube satellites.

1.3.9 PTB Primary Test Board. This board is used as the ultimate testing module for all three cycles of testing.

1.3.10 RTB: Redundant Test Board. This board was used as the pre-testing module for the primary test board.

1.3.11 Storage Temperature: The storage temperature (T_{stg}) refers to the temperature at which the device can be safely stored when the device is not powered[3].

1.3.12 Thermal Soak Duration: The thermal soak duration of a unit at the hot or cold extreme of a thermal cycle is the time that the unit is operating and its baseplate is continuously maintained within the allowed tolerance of the specified test temperature[4].

1.3.13 Temperature Stabilization: For thermal cycle and thermal-vacuum testing, temperature stabilization for a unit is achieved when the unit baseplate is within the allowed test tolerance on the specified test temperature, and the rate of change of temperature has been less than 3^{o}C per hour for 30 minutes[5]. For steady-state thermal balance testing, temperature stabilization is achieved when the unit having the largest thermal time constant is within 3^{o}C of its steady state value, as determined by numerical extrapolation of test temperatures, and the rate of change is less than 1^{o}C per hour[6].

1.3.14 Voltage Derating: The reduction of a voltage rating to extend the lifetime of an electric device or to permit operation at a high ambient temperature[7].

1.4 Language

Throughout the document, the following words shall have the meaning specified below:

"Shall": The use of this word expresses a mandatory requirement, which must be carried forward in lower level specifications. A "shall" statement describes a testable feature of the system.

"Should": This word expresses a preference.

"Must": This word describes a rather important feature of the system.

“Will”: Expresses an intended service. This describes a system feature.

“May or Can”: This expresses a permissible practice.

1.5 Documentation

With any test of this caliber, annotations, procedures, equipment lists, tolerances, software, test data, test log, test results and conclusion should be documented and recorded for further analysis and/or future work purposes. In this testing document, the above mentioned shall be clearly specified with sections entirely devoted to each individual category.

1.6 Test Procedure

This section includes all of the documentation requirements stated above except for the test data, results, and conclusions.

1.61 Test Abstract

The test will involve electrical circuitry. All components on the printed circuit board will include the expected operational voltages, impedance, frequencies, pulses and waveforms during the testing procedure. Electrical units will be cycled through all operational modes. The prototype sequencer electrical board will be tested to its performance requirements over the maximum expected range. If necessary, the unit may be powered off to facilitate reaching temperatures below the minimum temperature.

1.6.2 Testing Philosophy

The testing environment shall be set up to support collection of empirical data that accurately reflects realistic conditions. Furthermore, test methods and measured parameters shall be conducted in such a way to facilitate a realistic testing environment.

1.6.3 Test Log

The test log shall identify the number of personnel involved with this test. In addition, the test log will be completed at a high level of data precision. With this data, an analyst can reconstruct any significant times, testing events, anomalies, and any other significant findings.

1.6.3.1 There shall be at least two examiners responsible for conducting this test.

1.6.3.2 One examiner shall be in the vicinity of the testing area during the test progression. This is necessary because the thermal-vacuum apparatus is not automated. Therefore, manual operation of the unit is required to change phases, cycles, and temperatures in order to provide the proper test results.

1.6.3.3 The examiners will document the testing procedure after many of the preliminary tasks have been completed.

1.6.3.4 This testing procedure will not include the preliminary work that was done to create the board, the research, and the expected future work.

1.6.3.5 The examiners will remain on standby until the entire testing procedure is finished. At least one examiner will be present constantly for the testing.

1.6.3.6 The software package will record the data as the test progresses to the subsequent cycle. Therefore, it is not necessary for the authors to be present.

1.6.3.7 The examiners shall be present for the first cycle, one of the intermediate cycles, and the immediate cycles. This is to ensure that the vacuum chamber, primary test board, external prototype board, and the software are functioning as expected.

1.6.4 Duration

This section shall specify the MIL-HDBK-340A duration required for cycles and different stages of the cycles. In addition, this section shall detail the examiner created duration requirements for thermal-vacuum chamber pre-test, the proof-of-concept test, extreme cycle test, and the full acceptance test.

1.6.4.1 Cycle Standards

1.6.4.1.1 The minimum number of cycles involved with the test is 12.5[8]. The first and last test will be conducted using hot and cold temperatures during the first and last cycle[9]. After these tests are done, the unit will be returned to an ambient temperature in a vacuum[10]. The examiners shall not adhere to this rule for the purposes of this test. The modified requirements are stated further in the testing procedure.

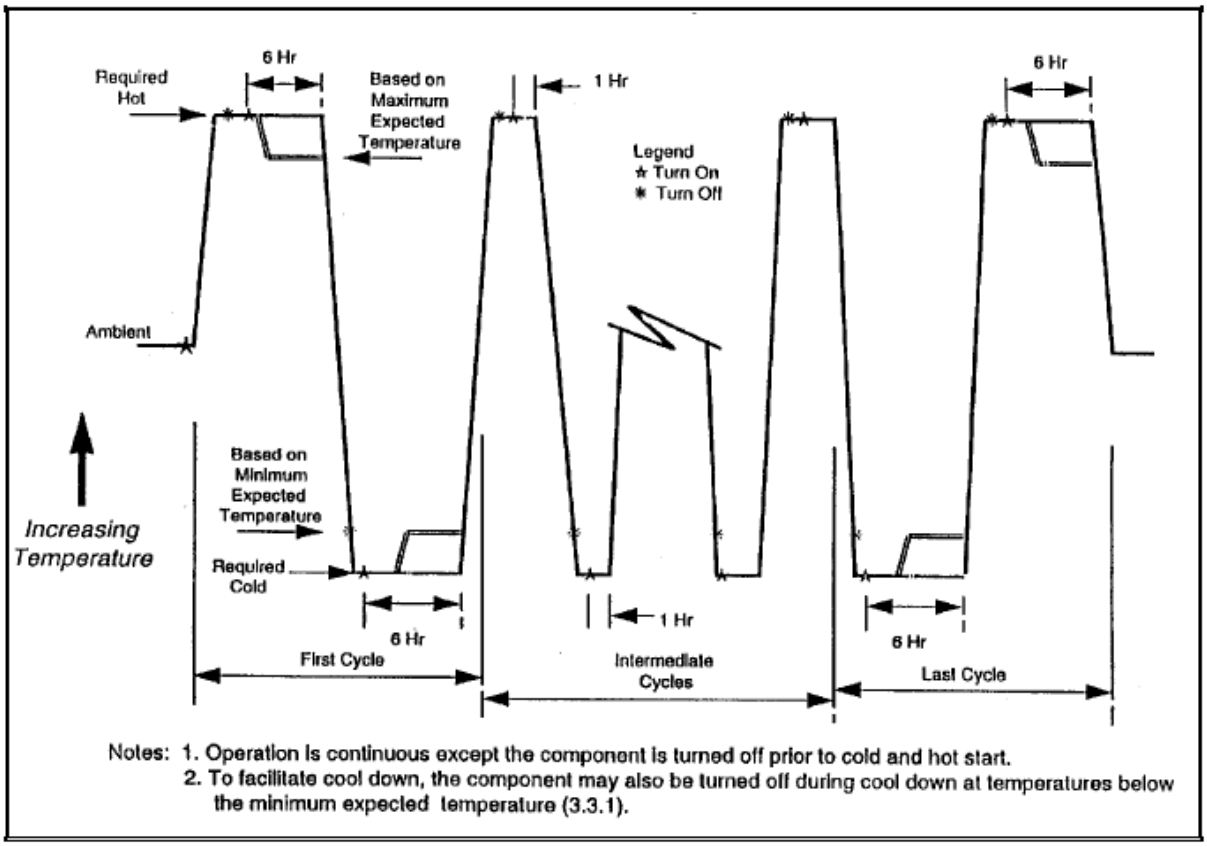
Required Testing		Unit			Vehicle	
		Acceptance (Table XIII)		Qualification (Table X)	Acceptance (Table XII)	Qualification (Table VIII)
		N_A[3]	N_{AMAX}[4]	N_Q[5]	N_A	N_Q[5,6]
Both:	TC[2]	8.5	17	53.5	4	10
	TV	4	8	25	1	3
Only	TV	1	2	6	4	13
Only	TC	12.5	25	78.5		

Notes:
1. Numbers of cycles correspond to temperature ranges in Table V.
2. Tests may be conducted in vacuum to be integrated with TV.
3. For tailoring: $N_A = 10(125/DT_A)^{1.4}$ for TC only and for the sum of TC and TV when both conducted.
4. $N_{AMAX} = 2N_A$, but can be changed to allow for more or less retesting.
5. $N_Q = 4N_{AMAX}(DT_A/DT_Q)^{1.4}$, assuming temperature cycling during missionor other service is insignificant; if significant, additional cycling will be required using the same fatigue equivalence basis.
6. $N_{AMAX} = N_A$, assuming that vehicle-level acceptance retesting will not be conducted.

Symbols:
- N_A = Required number of acceptance cycles.
- N_{AMAX} = Maximum allowable number of acceptance cycles, including retesting.
- N_Q = Required number of qualification cycles.

MIL-HDBK-340A Cycle Requirements[11]

1.6.4.1.2 Temperature soak durations will be a minimum of 6 hours at the hot and 6 hours at the cold temperature during the first and last cycle[12]. For the intermediate cycles, the soaks will be at least 1 hour long[13]. During soak periods, the unit will be turned off until the temperature stabilizes and then turned on[14]. For the purposes of this test, the examiners shall modify the cycle durations. This shall be detailed below.



MIL-HDBK-340A Cycle Description[15]

1.6.4.1.3 The last 100 hours of operation will be failure free[16]. The proctors will not adhere to this rule. First, the examiners shall not be conducting any tests that are longer than 45 hours. Therefore this rule does not apply. Second, the electrical board has commercial off the shelf (COTS) units that are not rated for space flight. On that note, the testers expect to see failures all throughout the testing profile including the final hours of testing.

1.6.4.1.4 For internally redundant units, the operating hours will consist of at least 150 hours of primary operation and at least 50 hours of redundant operation, the last 50 hours of each will be failure free[17]. The board used for this testing profile will not adhere to this rule because it does not have any redundant circuitry for redundant operations. The examiners do have a redundant test board. However, this board will not be used for the actual thermal-vacuum testing. In future iterations of the sequencer electrical board, the board will

have redundant circuitry. When these boards are created, they will be subjected to the above stated time standards for primary and redundant operations.

1.6.4.2 Cycling of the Test Board

1.6.4.2.1 The Thermal-Vacuum Chamber Pre-Test Duration

1.6.4.2.1.1 The examiners shall test the thermal-vacuum chamber alone for approximately 7 hours during the pre-testing phase.

1.6.4.2.1.2 There shall be one cycle consisting of a hot soaking period, a cold soaking period, temperature transition phases, and temperature stabilization phases specified further in the testing document.

1.6.4.2.1.3 The one cycle for this test shall start and finish respectively at an ambient temperature.

1.6.4.2.2 The Proof-of-Concept Test Duration

1.6.4.2.2.1 The examiners shall have a board that will reside inside a calibrated thermal-vacuum chamber for approximately 25 hours during a thermal-vacuum proof-of-concept test.

1.6.4.2.2.2 There shall be one cycle consisting of a hot soaking period, a cold soaking period, temperature transition phases, and temperature stabilization phases specified further in the testing document.

1.6.4.2.2.3 The one cycle for this test shall start and finish respectively at an ambient temperature.

1.6.4.2.3 The Extreme Cycle Test Duration

1.6.4.2.3.1 The examiners shall have a board that will reside inside a calibrated thermal-vacuum chamber for approximately 45 hours during a thermal-vacuum extreme cycle test.

1.6.4.2.3.2 There shall be one cycle consisting of a hot soaking period, a cold soaking period, temperature transition phases, and temperature stabilization phases specified further in the testing document.

1.6.4.2.3.3 The one cycle for this test shall start and finish respectively at an ambient temperature.

1.6.4.2.4 The Full Acceptance Test Duration

1.6.4.2.4.1 The examiners will have a board that will reside inside a calibrated thermal-vacuum chamber for approximately 95 hours during a full thermal-vacuum acceptance test. This test will not be done for the scope of the author's thesis.

1.6.4.2.4.2 There will be a total of 13 cycles consisting of hot soaking periods, cold soaking periods, temperature transition phases, and temperature stabilization phases specified further in the testing document.

1.6.4.2.4.3 The first and last cycles shall start and finish respectively at an ambient temperature.

1.6.4.3 Sampling the Test Board

1.6.4.3.1 The test board will run the program logic for the entire sequence until all eight circuits fire. When all eight circuits fire, this will be denoted as a set.

1.6.4.3.2 The set will fire in less than 10 seconds

1.6.4.3.3 Each firing of the circuit will be sampled by the appropriate software and will be visually displayed if applicable.

1.6.4.3.4 The set shall be sampled once every two minutes during all phases.

1.6.5 Temperature

The proof-of-concept, extreme thermal cycle, and acceptance tests shall be testing the temperatures of the entire testing system. Considering that the board is in a sealed chamber, the examiners will consider the temperature of the board and the temperature of the space inside the chamber as equal. Therefore, the temperature reference while conducting the test can be either the free space or the board itself.

1.6.5.1 Temperature Range

1.6.5.1.1 The range will encompass the maximum and minimum expected temperatures from the most temperature constrained components from the component temperature range table.

1.6.5.1.2 The range should be as large as practicable to meet environmental stress screening purposes[18]. A range of 105°C is recommended for acceptance testing.[19]

Required Testing	Unit	Vehicle	
	TC & TV	TC	TV
Acceptance (DT_A)	105°C[1]	≥ 50°C	note 3
Qualification (DT_Q)	125°C[2]	≥ 70°C[2]	note 4

Notes: 1 Recommended, but reduced if impracticable or increased if necessary to encompass operational temperatures (7.1.1).
2 $DT_Q = DT_A + 20°C$.
3 Governed by the unit that first reaches its hot or cold acceptance temperature limit.
4 Like note 3, but for qualification temperature limit.

Symbols: DT_A = Acceptance temperature range.
DT_Q = Qualification temperature range.

MIL-HDBK-340A Acceptance and Qualification Temperature Ranges[20]

1.6.5.1.3 The proctors of this test will satisfy the MIL-HDBK-340A temperature range requirement on the proof-of-concept, extreme cycle, and full acceptance tests.

1.6.5.1.4 The range of the proof-of-concept test shall be 120°C

1.6.5.1.5 The range of the extreme cycle test shall be 240°C

1.6.5.2 The transitions between cold and hot temperatures should be at an average rate of 3oC to 5oC per minute and will not be slower than 1oC per minute[21]. The examiners shall meet this requirement. However, the examiners may not meet the transition between hot and cold temperatures based on the criteria of the thermal-vacuum chamber. This topic will be discussed in detail in the "Calibration and Test Accuracy" section of this document.

Component	Temperature			
	Storage		Operating	
	Minimum	Maximum	Minimum	Maximum
2N2222A NPN Transistor[22]	-65	175	*	175 (Junction)
594D Tantalum Capacitor[23]	*	*	-55	85 (125 Voltage Derating)
ECJ Ceramic Capcitor[24]	*	*	-55	125
DO-214AB Schottky Rectifier[25]	-65	150	-65	150 (Junction)
ERJ Chip Resistor[26]	*	*	-55	155
JSM1a Panasonic Relay[27]	*	*	-40	85
G5RL Relay[28]	*	*	-40	85
JQ1aP Relay[29]	*	*	-40	85
LM2678 Voltage Regulator[30]	*	*	-45 (Junction)	125 (Junction)
MAX 4427 MOSFET[31]	*	*	-55	125 (150 Chip Temp)
MAX 6630 Temperature Sensor[32]	*	*	-55	125 (150 Extended Range)
JW5 NUD3112 Relay Driver[33]	*	*	-40	85
Toroid Power Inductor[34]	*	*	-40	130
SOD-123 Schottky Rectifier[35]	*	*	-65	125

Component Temperature Range Table

1.6.5.4 The Vacuum Chamber Pre-Test Thermal Constraints

1.6.5.4.1 There are no thermal constraints in this section. The pre-test is primarily for verification of the proper operation of vacuum chamber equipment.

1.6.5.4.2 Although there are no constraints for this pre-test, there are limitations that the examiners have implemented for the testing. The pre-test shall have a temperature range of 8^{o}C to 43^{o}C to test the thermal-vacuum chamber functionality.

1.6.5.5 The Proof-of-Concept and Full Acceptance Tests Thermal Constraints

1.6.5.5.1 These tests shall be based on the components with the least temperature ranges on the component temperature range table.

1.6.5.5.2 The temperature variation for the J-SM1 Relay, JQ1-aP Relay, and the JW5 NUD3112 Relay Driver will be the baseline range for these tests.

1.6.5.5.3 The examiners shall use the temperature range of -40oC to 85oC as the temperature range for both tests

1.6.5.6 The Extreme Thermal Cycle Test Thermal Constraints

1.6.5.6.1 This test shall be based on the most extreme temperature components listed on the component temperature range table.

1.6.5.6.2 The storage temperature for the 2N2222A NPN Transistor shall be used as the baseline temperature range for the test.

1.6.5.6.3 The examiners shall use the temperature range of -65oC to 175oC as the temperature range for both tests

Thermal Vacuum*	1 cycle, -44 to +61°C (7.1.1). Vacuum at 13.3 millipascals (10^{-4} Torr).	4 cycles, -44 to +61°C (7.2.8). Same pressure as for units.
Thermal Cycle*	12.5 cycles, -44 to +61°C.	See 7.2.7.
Combined Thermal Vacuum and Cycle*	8.5 thermal cycles and 4 thermal vacuum cycles, -44 to +61°C.	See 7.2.7.

MIL-HDBK-340A Thermal and Duration Requirements[36]

1.6.6 Pressure

This section delineates the appropriate pressures that shall be used during thermal/vacuum testing. For the purposes of this test, each testing cycle will be in a vacuum to mimic a microgravity environment.

1.6.6.1 The pressure will be reduced from atmospheric to 13.3 millipascals (10^{-4} Torr) for on-orbit simulation, or to the functionally appropriate reduced pressure, at a rate that simulates the ascent profile, to the extent practicable[37]. For launch vehicle units, the vacuum pressure will be modified to reflect an altitude consistent with the maximum service altitude[38]. Currently, the launch providers have not issued the necessary information to create an accurate vacuum profile for testing[39]. On that note, the test will not reflect the appropriate ascent profile. However, the proctors shall attempt to create an accurate reduced atmospheric environment equivalent to the specification.

1.6.6.2 For units that are proven to be free of vacuum related failure modes, the thermal-vacuum acceptance test may be conducted at ambient. Considering that the test board has not been proven to be free of vacuum related failure modes,

the thermal-vacuum acceptance test will be conducted at the specified number of vacuum modes.

1.6.6.3 For testing purposes, ambient pressure shall be considered 760 Torr[40]

1.6.7 Circuitry and Outputs

This section shall discuss the requirements for the electrical operation of the test board while it is being tested.

1.6.7.1 The board will have eight dissimilar circuits that produce eight identical outputs.

1.6.7.2 The outputs will simulate the opening of P-POD doors.

1.6.7.3 Actual P-POD doors are designed to open at 120 milliseconds given a 28 volt and 2 amp input[41]. The programming logic and the components on the board are setup so that each circuit fires sequentially at a rate of 250 milliseconds per circuit.

1.6.7.4 Each of the eight circuits contains different components to accomplish the same mission.

1.6.7.5 The outputs of the circuits can be illuminated by LEDs during the pre-test phases outside of the vacuum chamber on both the primary and redundant test boards.

1.6.7.6 The outputs of the circuits shall be indicated by the Stamp editor and the Excel spreadsheet during testing.

1.6.7.7 The circuitry is expected to fail during the vacuum chamber testing.

1.6.7.8 The output variances are expected to change during the vacuum chamber testing.

1.6.8 Supplementary Requirements

A functional and monitoring test will be performed before, during, and after the unit test to detect equipment anomalies.

1.6.9 Computer Software

1.6.9.1 Windows Operating System

1.6.9.2 Parallax Basic Stamp Editor

The Stamp editor shall store the program logic, send the signals to program the basic Stamp on the test boards, and verify proper operation of the basic Stamp.

1.6.9.3 Microsoft Office Excel 2003 (or newer versions)

The Excel spreadsheet shall record all test data at the appropriate sampling rate. The spreadsheet shall contain at least the circuit being fired, the current time, a pass/fail decision to determine proper/improper operation respectively, a temperature reading, and the voltage of the respective circuits being fired.

1.6.10 Calibration and Test Accuracy

This section shall specify how well the system is calibrated and provide some thumb rules for testing accuracy.

1.6.10.1 Thermal Calibration and Test Accuracy

1.6.10.1.1 According to the engineering staff at NPS, the integrated thermal-vacuum chamber thermocouples are not functioning properly[42]. Therefore, the thermal integrated circuit devices mounted on the primary test board shall be used to provide temperature telemetry feedback to the appropriate software.

1.6.10.1.2 The thermal sensor integrated circuits mounted on the test boards have a $^{+}$/- 1^{o}C tolerance[43].

1.6.10.1.3 According to Mr. Ron Phelps, the resident expert on thermal-vacuum chamber operations, the chamber will not meet MIL-HDBK-340A standards for heat up and cool down rates [44].

1.6.10.1.4 According to Mr. Phelps, the average rate of cooling on a recent test was less than one-tenth of a degree per minute [45]. This value shall be used for the purposes of thermal cycling schedule.

1.6.10.1.5 The test shall be conducted similar to the MIL-HDBK-340A standards. However, the test shall be modified to fit the author's thesis fulfillment needs.

1.6.10.1.6 Visual inspection of the thermal-vacuum chamber indicates that the thermocouple displays have a tolerance of $^{+}$/- 0.5 degree.

1.6.10.1.7 The operator must acquire a cold plate and apply liquid nitrogen to get colder than -60^{o}C[46]

1.6.10.2 Visual inspection of the thermal-vacuum chamber pressure indicator reveals that the pressure is accurate to $^{+}$/- 300 meters.

1.6.11 Acquire Materials

1.6.11.1 The examiner should gather the necessary materials specified on the Tools List table.

1.6.11.2 The examiner should verify all the components that are going to be tested are mounted on the testing board in a proper electrical configuration. These components are displayed on this document's Parts List table.

1.6.11.3 Examining for proper component placement may require examining schematics, component datasheets, and third party verifications.

1.6.11.4 In addition to the above mentioned tables, for this procedure, the examiners chose to make a duplicate board with duplicate components. The primary and redundant boards will be used at different points of the testing process.

1.6.12 Test Equipment

1.6.12.1 Parts List

Manufacturer	Part#	DigiKey#	Description	Qty.
National Semiconductor	LM2678S-12/NOPB	LM2678S-12-ND	IC REG SIMPLE SWITCHER TO-263-7	3
Pulse	P0849NL	553-1122-ND	INDUCTOR 33UH 5A 260KHZ KLIPMNT	3
AVX Corporation	TPSD107K016R0125	478-1778-1-ND	CAP TANT LOESR 100UF 16V 10% SMD	3
Vishay/Sprague	594D156X0050R2T	718-1008-1-ND	CAP TANT 15UF 50V 20% SMD	9
Vishay/General Semiconductor	SSC54-E3/57T	SSC54-E3/57TGICT-ND	DIODE SCHOTTKY 5A 40V SMC	3
STMicroelectronics	2N2222A	497-2598-ND	TRANSISTOR NPN 75V 0.6A TO-18	6
ON Semiconductor	NUD3112LT1G	NUD3112LT1GOSCT-ND	IC INDUCTIVE LOAD DRVR 14V SOT23	6

Manufacturer	Part#	DigiKey#	Description	Qty.
Maxim Integrated Products	MAX4427ESA+	MAX4427ESA+-ND	IC MOSFET DRV DUAL NONINV 8-SOIC	6
Panasonic - ECG	ECJ-2VB1H103K	PCC103BNCT-ND	CAP 10000PF 50V CERM CHIP 0805	30
Panasonic - ECG	ECJ-3VB1H104K	PCC104BCT-ND	CAP .1UF 50V CERM CHIP 1206 X7R	15
Panasonic - ECG	ERJ-8ENF1002V	P10.0KFCT-ND	RES 10.0K OHM 1/4W 1% 1206 SMD (200)	1
Panasonic - ECG	ERJ-8ENF1001V	P1.00KFCT-ND	RES 1.00K OHM 1/4W 1% 1206 SMD (200)	1
Tyco Electronics	OJE-SH-112HM,000	PB876-ND	RELAY GP SPST-NO 10A 12VDC	6
Panasonic Electric Works	JQ1AP-12V-F	255-2071-ND	RELAY PWR HI-CAP 200MW 12VDC PCB	6
Omron Electronics Inc-ECB Div	G5RL-1A-E-HR DC12	Z2580-ND	RELAY PWR SPST 16A 12VDC PCB	6
Panasonic Electric Works	JSM1A-12V-4	255-2223-ND	RELAY AUTO 10A 12VDC SEALED PCB	6
Texas Instruments	CD74HC4067M	296-9225-5-ND	IC MUX/DEMUX ANALOG HS 24-SOIC	6
Parallax Inc	BS2-IC	STAMP2-ND	Basic Stamp II Module	3

Test Board Parts List

1.6.12.2 Tools List

Quantity	Tool Description
1	Agilent E3632A DC Power Supply
1	PC with Windows Operating System and Microsoft Office
1	Parallax Stamp Editor and Prototype Board
1	22 Gauge Wire Spool
1	Tenney Thermal-Vacuum Chamber and Harnessing
1	Soldering Iron and Spool of Solder
1	Spool of Solder
1	Wire Stripper
1	Wire Cutter
1	9 Pin DB-9 Male Connector
1	25 Pin DB-9 Male Connector
1	50 Pin DB-9 Male Connector

Quantity	Tool Description
1	Vacuum Chamber Electronics Interface Document
1	Thermal-Vacuum Port Harness Document
8	6.2K Ohm Resistor
8	10K Ohm Resistor

Tools List

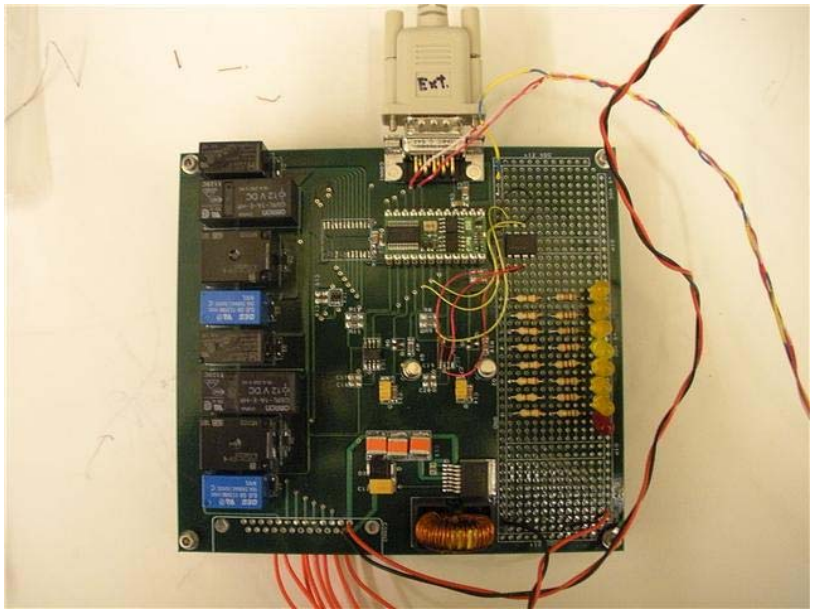
1.6.13 Functional Pre-Test of the Redundant Board

This section shall detail the requirements, pre-test procedure, installation, and operation of the redundant test board.

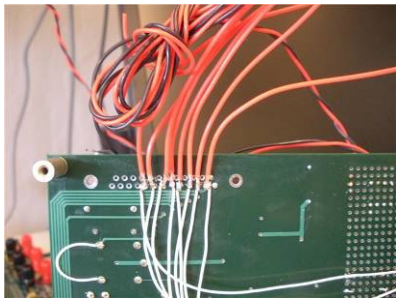
1.6.13.1 The examiner shall verify the proper operation of the electrical board by performing a functional test and examining the results. The examiners of this test use a redundant test board to complete this procedure. This board will be used as the pre-test working model because the examiners do not want to corrupt the actual test board used for thermal-vacuum testing.

1.6.13.2 The redundant test board will have a power supply, a communications interface, and connections to a prototype board for functional verification.

1.6.13.3 The examiners used a DB-9 male and female connector for the communications interface. The examiners used the Agilent power supply to deliver the power to the board. Finally, the authors used eight 22 gauge wire to connect the redundant test board to the prototype board in order to verify proper operation. These wires are connected to the outputs of the circuitry that simulate the opening of eight poly picosatellite orbital deployer (P-POD) units.

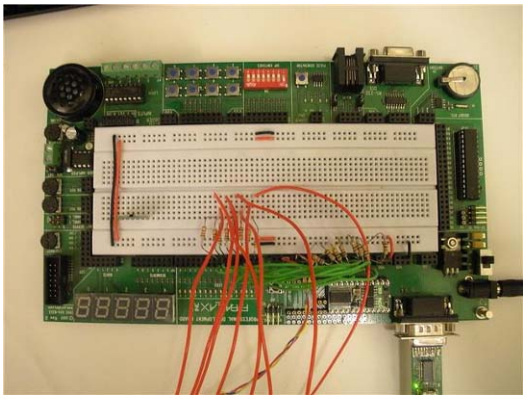


Redundant Test Board (RTB)



RTB 8 Connections to Prototype Board

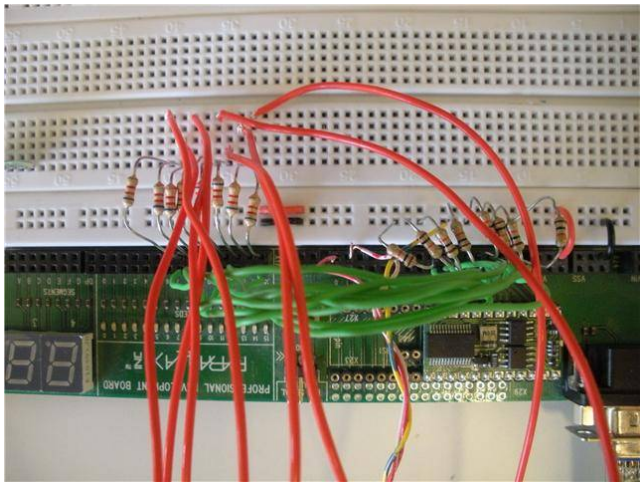
1.6.13.4 The outputs of the 8 connection points of the redundant test board will be connected to the Parallax prototype board for functional verification. Using the prototype board is not necessary for testing purposes. There are many other ways a functional test could have been administered. Simply put, using the prototype board is one way that the examiners chose to use. Since the use of this board is not mandatory, necessary components, communication interfaces, and any additional wiring for the proper operation of this prototype board are not included in this procedure. However, it is still necessary to for the author to note the role this hardware plays in the pre-test.



Parallax Prototype Board

1.6.13.5 Voltage dividers will be used to step down the voltage from 28 volts to 3.2 volts for proper Stamp controller operation. The Parallax prototype board contains an integrated 470 ohm resistor network that must be taken into consideration when creating voltage dividers. In addition, the examiners chose eight 6.2K ohm resistors to provide the proper voltage drop for the basic Stamp controller operation.

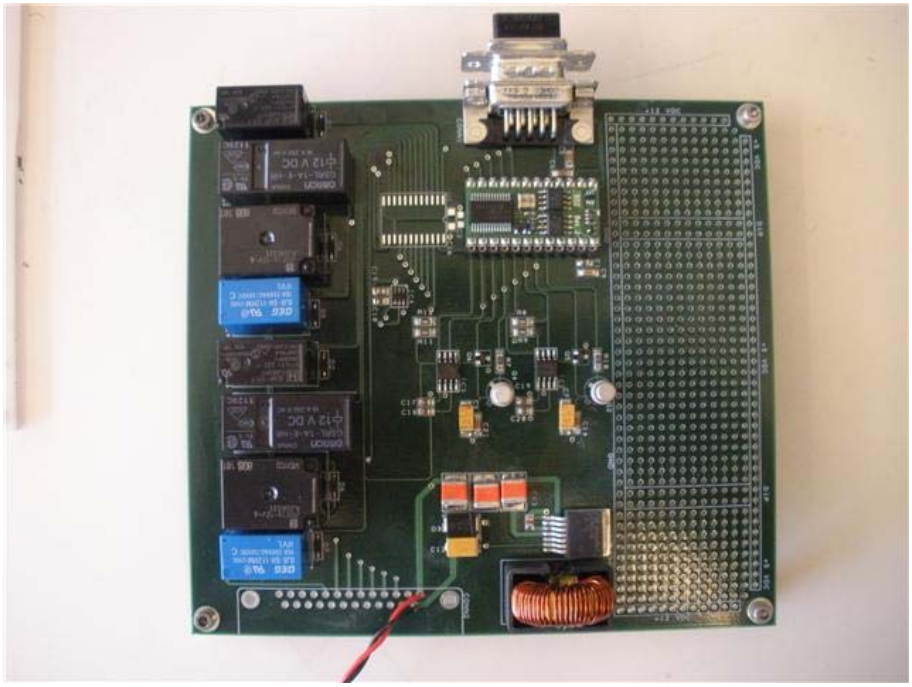
1.6.13.6 Certain visual verifications will be used for proper operations. If the electrical circuitry is properly configured, light emitting diodes (LEDs) corresponding to each of the pin-outs and wiring configuration will light up in respect to the programming sequence. In addition, the examiner could verify proper function by reading the telemetry feedback displayed on the associated Stamp editor display or the Microsoft Excel spreadsheet. Finally, the examiner could use a voltmeter to verify the appropriate voltages exist at specific nodes on the board.



RTB Connection to Prototype Board Voltage Divider

1.6.14 Preparation for Vacuum Chamber Entry

1.6.14.1 Acquire the Primary Test Board



Before Testing Primary Test Board

1.6.14.2 Administer the pre-testing procedure stated above for proper functional verification of the primary test board. Note that no LEDs are installed on this test board. This test board will not require LEDs because there will be no visual verification of the board itself when it is inside the vacuum chamber.

1.6.14.3 Clean the Primary Test Board

The examiner will use the proper cleaning procedures, solutions, and sanitary cloths to remove oil and debris from the board before testing. Oil and debris can significantly affect thermal-vacuum testing results; therefore, it is necessary to have a clean board.

1.6.14.4 Don the appropriate gloves to handle the board for the rest of the procedure

1.6.14.5 Bring the primary test board and associated equipment to stage next to the vacuum chamber.

1.6.15 Interfacing with the Vacuum Chamber

1.6.15.1 Open the thermal-vacuum chamber door. Do not touch the gasket. Touching the gasket will cause the door not to seal properly and/or add oil and debris to the chamber[47].

1.6.15.2 Attach the ribbon cable extending from primary test board to the 50 pin connector inside the chamber. This connection provides the power and communication between both the test board and the prototype board.

Thermal-Vacuum Chamber and Internal Connectors

1.6.15.3 Attach the external harnessing of the vacuum chamber to the communication board. This requires the male 25 pin connector to attach to the communication board and then to attach to the external harnessing.

Thermal-Vacuum Chamber External Harness

1.6.16 Vacuum Chamber Connector Test

1.6.16.1 Start up the Windows operating system along with the Parallax Basic Stamp Editor and a new Microsoft Excel spreadsheet.

1.6.16.2 Initial setup (For the Proof-of-Concept test only): Load the master and slave programs on the communication board and PTB respectively.

1.6.16.3 Final setup (For the Extreme Thermal Cycle test only): Load the slave program on the PTB and use the communication as LED relay actuation visual indication.

1.6.16.4 Execute the program and look for visual indication on the Stamp Editor and the Excel Spreadsheet. Once again, these are the only indications that one can see considering the primary test board has no light indications.

1.6.16.5 One should see eight relays appearing sequentially on the spreadsheet in discrete time intervals. In addition one should see time lapses and a temperature readout. Once these indications are displayed, the examiner will know that the device, internal board components, connectors inside and outside of the vacuum chamber are functioning properly. Once the system is verified, actual testing can begin.

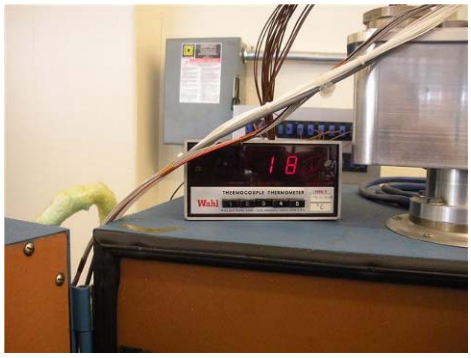
1.6.17 Common Practices among all Thermal-Vacuum Testing

1.6.17.1 Follow the "Tenney Space Jr." guide for all testing purposes. The procedures outline in this document shall be followed verbatim.

1.6.17.2 Refer to the "Tenney Space Jr." guide for descriptions of thermal-vacuum chamber components, preconditioning, calibration, and precautionary information.

1.6.17.3 Operate and observe the following instruments and meters during heat ups and cool downs.

TempTenn Instrument and Meter Panel



Thermocouple Thermometer

1.6.17.4 Making a Space Run-Turn off Safety Switch[48]

1.6.17.4.1 Inspect the door, penetrations and ionizations gauge glass tube for tightness

1.6.17.4.2 Turn on the safety switch

1.6.17.4.3 Close the circuit breakers

1.6.17.4.4 Turn on the mechanical pump

1.6.17.4.5 Pump the chamber with the mechanical vacuum pump until the pressure falls to 200 microns or less as indicated on the chamber thermocouple gauge.

Thermal-Vacuum Chamber Pressure Meter

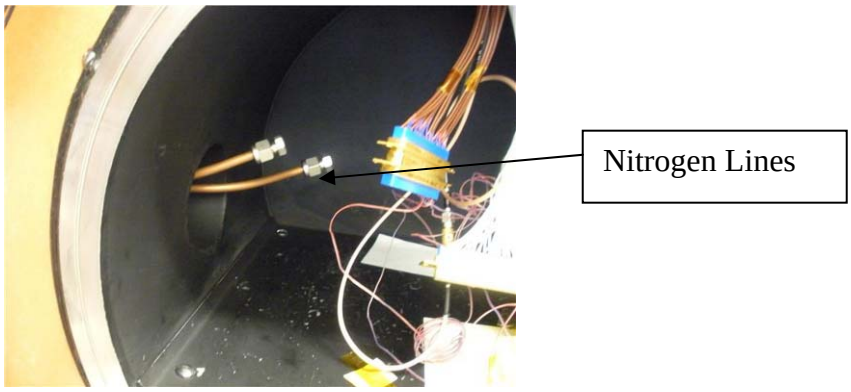
1.6.17.4.6 Turn on the turbo V200 turbo pump controller.

Turbo Pump Controller

1.6.17.4.7 Turn on the cold trap.

1.6.17.4.8 If you want absolute ultimate altitude, feed liquid nitrogen to the cold trap and shut off the cold trap switch.

External Nitrogen Tank Used For Ultimate Altitude



Nitrogen Connections inside Chamber

1.6.17.4.9 Select desired temperature on the TempTenn

1.6.17.5 Returning to Site Altitude[49]

1.6.17.6 Shut off the cold trap switch or turn off the liquid nitrogen if it is being used.

1.6.17.7 Turn off the Turbo U200 pump (keep the mechanical pump running).

1.6.17.8 Allow the Turbo U200 to stop. One can tell when the pump is approaching a full stop by listening to the pump to whir down. Do not stop the mechanical pump yet.

1.6.17.9 If the shell is colder than ambient, warm it a little above ambient.

1.6.17.10 Check the pressure meter for visual indication for a new equilibrium pressure. Once this pressure is reached, one will see the pressure remain almost

stationary. Along with the listening for audible cues, one can tell that the turbo pump has stopped by this stationary pressure indication.

1.6.17.11 Bleed in clean gaseous nitrogen until the mechanical pump gurgles. Finally, shut down the mechanical pump.

1.6.17.11.1 Crack open the main tank valve to allow the flow of nitrogen gas.

1.6.17.11.2 Crack open the line valve to allow the nitrogen line to be pressurized.

1.6.17.11.3 Adjust the line pressure instrument to a little over ambient pressure (approximately 20 $^{lbs.}/_{in.^2}$)

1.6.17.11.4 Attach the nitrogen line to the connecting port called "Vent" on the TempTenn panel

Nitrogen Tank Used to Return Chamber to Ambient

1.6.17.11.5 Turn off all switches on the TempTenn, then turn off the main circuit breaker, then turn the safety switch to off.

1.6.18 The Pre-Test of the Thermal-Vacuum Chamber

This section shall detail the pre-test procedure to verify the thermal-vacuum chamber's operational capabilities.

1.6.18.1 The thermal-vacuum chamber will be tested prior to the installation of the primary test board.

1.6.18.2 This test will familiarize the examiners with the heat up rate, cool down rate, overall functioning properties, and any anomalies associated with the thermal-vacuum chamber.

1.6.18.3 The thermal-vacuum chamber has variable heat up and cool down rates. Therefore, the time and temperature values given in this section shall be treated as expected values based on empirical standards and the guidelines stated previously in this document.

1.6.18.4 Due to the thermal-vacuum chamber's cooling rate, the thermal-vacuum chamber pre-test will neither follow the format of the MIL-HDBK-340A standards nor will it follow the same format as the proof-of-concept and extreme thermal cycle tests. It would take a superfluous amount of time to administer the test by the standards. Cooling then subsequently heating the system will maximize the examiners resources. Therefore, the examiners will follow this modified testing approach. Furthermore, the examiners feel this is satisfactory considering that this is simply an equipment familiarization test.

1.6.18.5 The test shall be conducted as follows:

1.6.18.5.1 Thermal-Vacuum Chamber Pre-Test Table

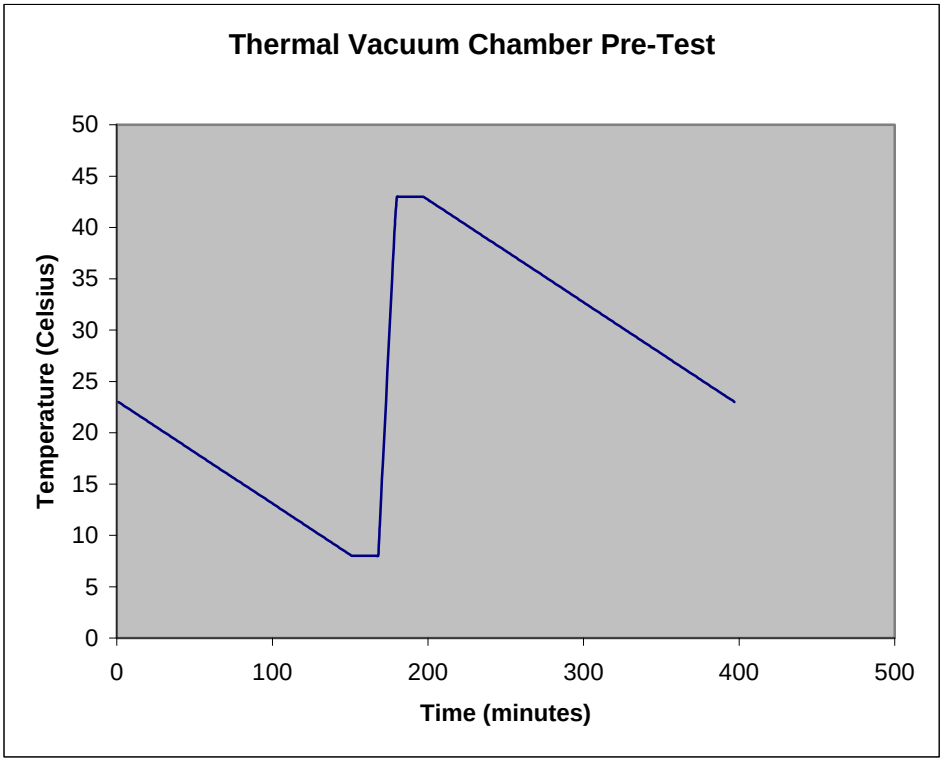
The test will progress down the table from top to bottom within the cycle.

Thermal-Vacuum Chamber Pre-Test with Vacuum			
Phase	Temperature (^{o}C)	Duration (minutes)	Accumulated Time (minutes)
Ambient to Cold Soak	23 to 8	151	151
Temperature Stabilization Cold	8	6	157
Cold Soak	8	10	167
Transition to Hot Soak	8 to 43	13	180
Temperature Stabilization Hot	43	6	186
Hot Soak	43	10	196
Transition to Ambient	43 to 23	201	397

Total Cycle Testing Time
6 hours 36 minutes

Expected Thermal-Vacuum Chamber Pre-Test Cycle Description Table

1.6.18.5.2 Thermal-Vacuum Chamber Pre-Test Chart



Expected Thermal-Vacuum Chamber Pre-Test Graph

1.6.19 Test Commencement

1.6.19.1 This actual testing of the primary test board begins in this section.

1.6.19.2 The test will commence in consecutive cycle order. In addition, the test will progress down the table from top to bottom within each cycle. Once again, manual operation of the chamber is necessary to change phases, cycles, and temperatures.

1.6.19.3 The thermal-vacuum chamber has variable heat up and cool down rates. Therefore, the time and temperature values given in this section shall be treated as expected values based on empirical standards and the guidelines stated previously in this document.

1.6.19.4 Proof-of-Concept Testing

1.6.19.4.1 Proof-of-Concept Thermal Cycle Test Tables

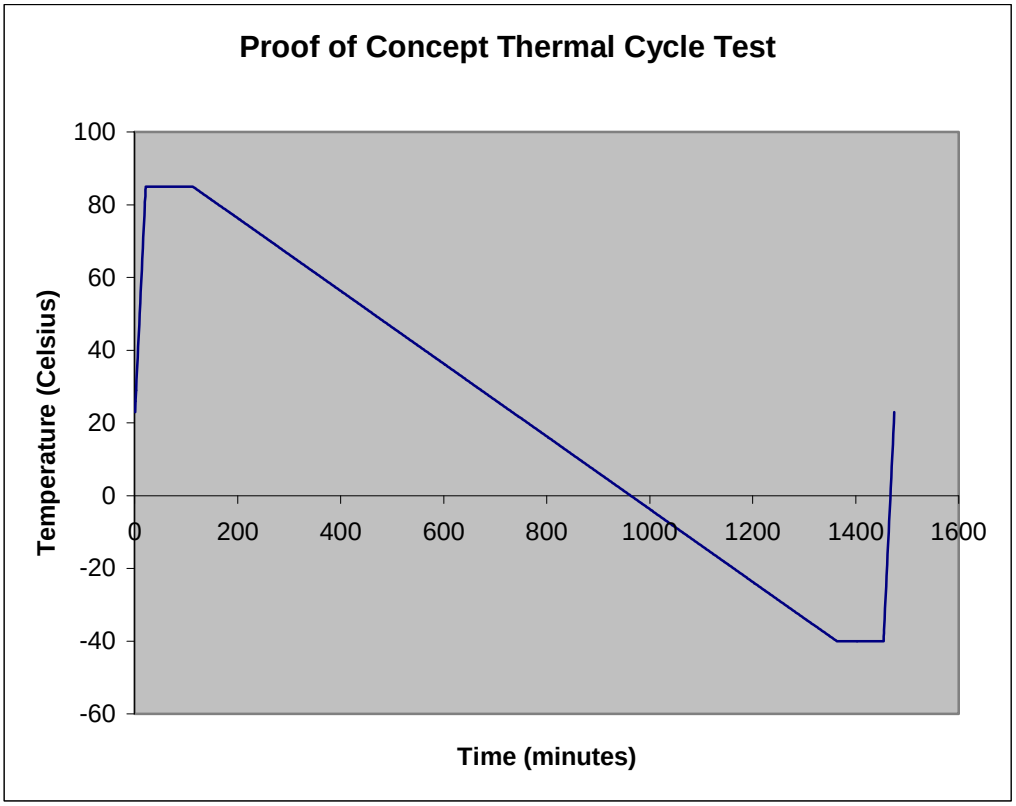
Proof-of-Concept Cycle with Vacuum

Phase	Temperature (°C)	Duration (minutes)	Accumulated Time (minutes)
Ambient to Hot Soak	23 to 85	22	22
Temperature Stabilization Hot	85	30	52
Hot Soak	85	60	112
Transition to Cold Soak	85 to -40	1251	1363
Temperature Stabilization Cold	-40	30	1393
Cold Soak	-40	60	1453
Transition to Ambient	-40 to 23	22	1475

Total Cycle Testing Time
24 hours 35 minutes

Expected Proof-of-Concept Thermal Cycle Test Description Table

1.6.19.4.2 Proof-of-Concept Thermal Cycle Test Chart



Expected Proof-of-Concept Thermal Cycle Test Graph

1.6.19.5 Extreme Cycle Testing

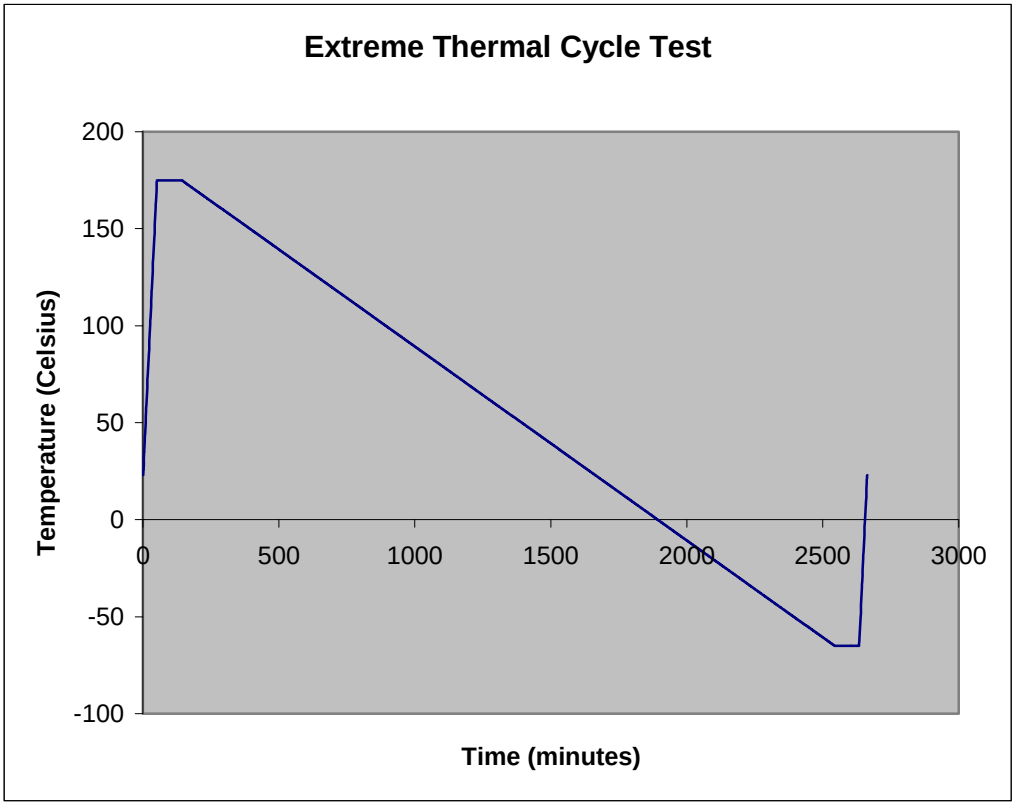
1.6.19.5.1 Extreme Cycle Test Tables

Extreme Cycle with Vacuum			
Phase	Temperature (^{o}C)	Duration (minutes)	Accumulated Time (minutes)
Ambient to Hot Soak	23 to 175	52	52
Temperature Stabilization Hot	175	30	82
Hot Soak	175	60	142
Transition to Cold Soak	175 to -65	2401	2543
Temperature Stabilization Cold	-65	30	2573
Cold Soak	-65	60	2633
Transition to Ambient	-65 to 23	31	2664

Total Cycle Testing Time
44 hours 24 minutes

Expected Extreme Thermal Cycle Test Description Table

1.6.19.5.2 Extreme Cycle Test Chart



Expected Extreme Thermal Cycle Test Graph

1.6.19.6 Full Acceptance Testing (For future work)

1.6.19.6.1 Cycle 1

Cycle 1: First Cycle Parameters (No Vacuum)			
Phase	Temperature (^{o}C)	Duration (minutes)	Accumulated Time (minutes)
Ambient to Hot Soak	23 to 85	22	22
Temperature Stabilization Hot	85	30	52
Hot Soak	85	360	412
Transition to Cold Soak	85 to -40	43	455
Temperature Stabilization Cold	-40	30	485
Cold Soak	-40	360	845
Transition to Hot Soak	-40 to 85	43	888

Full Acceptance Testing Cycle 1

1.6.19.6.2 Cycle 2-5

Cycle 2 - 5: Cycle Parameters (No Vacuum)			
Phase	Temperature (^{o}C)	Duration (minutes)	Accumulated Time (minutes)
Temperature Stabilization Hot	85	30	30
Hot Soak	85	60	90
Transition to Cold Soak	85 to -40	43	133
Temperature Stabilization Cold	-40	30	163
Cold Soak	-40	60	223
Transition to Hot Soak	-40 to 85	43	266
Temperature Stabilization Hot	85	30	296
Hot Soak	85	60	356

Full Acceptance Testing Cycle 2-5

1.6.19.6.3 Cycle 6-9

Cycle 6 - 9: Cycle Parameters (Vacuum)			
Phase	Temperature (^{o}C)	Duration (minutes)	Accumulated Time (minutes)
Temperature Stabilization Hot	85	30	30
Hot Soak	85	60	90
Transition to Cold Soak	85 to -40	43	133
Temperature Stabilization Cold	-40	30	163
Cold Soak	-40	60	223
Transition to Hot Soak	-40 to 85	43	266
Temperature Stabilization Hot	85	30	296
Hot Soak	85	60	356

Full Acceptance Testing Cycle 6-9

1.6.19.6.4 Cycle 10-12

Cycle 10 - 12: Cycle Parameters (No Vacuum)			
Phase	Temperature (°C)	Duration (minutes)	Accumulated Time (minutes)
Temperature Stabilization Hot	85	30	30
Hot Soak	85	60	90
Transition to Cold Soak	85 to -40	43	133
Temperature Stabilization Cold	-40	30	163
Cold Soak	-40	60	223
Transition to Hot Soak	-40 to 85	43	266
Temperature Stabilization Hot	85	30	296
Hot Soak	85	60	356

Full Acceptance Testing Cycle 10-12

1.6.19.6.5 Cycle 13

Cycle 13: Last Cycle Parameters (No Vacuum)			
Phase	Temperature (°C)	Duration (minutes)	Accumulated Time (minutes)
Transition to Cold Soak	85 to -40	43	43
Temperature Stabilization Cold	-40	30	73
Cold Soak	-40	360	433
Transition to Hot Soak	-40 to 85	43	476
Temperature Stabilization Hot	85	30	506
Hot Soak	85	360	866
Transition to Ambient	23	22	888

Full Acceptance Testing Cycle 13

1.6.19.6.6 Total Cycle Testing Time

Total Cycle Testing Time
94 hours 52 minutes

Total Cycle Testing Time

1.6.20 Test Conclusion

The examiners shall restore all testing equipment and support to the condition they were in originally.

1.7 Test Data

1.7.1 The examiners shall retrieve, record, and save the data all throughout the testing process.

1.7.2 The examiner will conduct an analysis of all the testing data that was retrieved during the testing process.

1.7.3 The test data should be maintained in quantitative form to permit the evaluation of performance under the various specified test conditions.

1.7.4 The test data should also be compared across major test sequences for trends or evidence of anomalous behavior.

1.7.5 A summary of the test results should be documented in test reports.

1.7.6 The test report should detail the degree of success in meeting the test objectives.

1.8 Analysis Results and Conclusions

This section will be covered in the NPSCuL-Lite Prototype Sequencer Thesis Chapter, “Thermal-Vacuum Test.”

NOTES

1. <http://www.altera.com/support/kdb/solutions/963.html> Altera Corporation, 2009. 1 Jan. 2009.
2. Ibid
3. Ibid
4. MIL-HDBK-340A: Department of Defense Handbook Test Requirements for Launch, Upper-Stage, and Space Vehicles Vol I: Baselines. Defense Standardization Program Office (DLSC-LM): Los Angeles, 1999.
5. Ibid
6. Ibid
7. <http://www.altera.com/support/kdb/solutions/963.html> Altera Corporation, 2009. 1 Jan. 2009
8. MIL-HDBK-340A: Department of Defense Handbook Test Requirements for Launch, Upper-Stage, and Space Vehicles Vol I: Baselines. Defense Standardization Program Office (DLSC-LM): Los Angeles, 1999.
9. Ibid
10. Ibid
11. Ibid
12. Ibid
13. Ibid
14. Ibid
15. Ibid
16. Ibid
17. Ibid
18. Ibid
19. Ibid
20. Ibid
21. Ibid
22. "2N2219/22A High Speed Switches." E-mail sent to the author. STMicroelectronics, 2003. Naval Postgraduate School, Monterey. 1 Apr. 2009.
23. "Solid Tantalum Chip Capacitors Tantamount Conformal Coated, Maximum CV, Low ESR." Vishay Sprague, 2008. 1 Apr. 2009. <www.vishay.com>
24. "Multilayer Ceramic Capacitors (For General Electronic Equipment)." E-mail sent to the author. Panasonic, 2009. Naval Postgraduate School, Monterey. 1 Apr. 2009.
25. "Schottky Rectifiers." STMicroelectronics, 2002. 1 Apr. 2009. <http://www.st.com>
26. "Precision Thick Chip Film Resistors." E-mail sent to the author. Panasonic, 2007. Naval Postgraduate School, Monterey. 1 Apr. 2009.
27. "JS-M Relays." E-mail sent to the author. Matsuhita Electric Works, Ltd. Naval Postgraduate School, Monterey. 1 Apr. 2009.
28. "PCB Relay G5RL." Omron Electronic Components, LLC.:Schaumburg, 2008. 1 Apr. 2009. <http://www.components.omron.com>

29. "High Electrical & Mechanical Noise Immunity Relay: JQ Relays." E-mail sent to the author. Matsuhita Electric Works, Ltd. 1 Apr. 2009.
30. "LM2678 Simple Switcher High Efficiency 5A Step-Down Voltage Regulator." E-mail sent to the author. National Semiconductor Corporation, 2008. Naval Postgraduate School, Monterey. 1 Apr. 2009.
31. "Maxim Dual High-Speed 1.5A MOSFET Drivers." E-mail sent to the author. Maxim Integrated Products, Inc., 2006. Naval Postgraduate School, Monterey. 1 Apr. 2009.
32. "Maxim 12-Bit +Sign Digital Temperature Sensors with Serial Interface." Maxim Integrated Products: Sunnyvale, 2005
33. "NUD3112 Integrated Relay, Inductive Load Driver." Semiconductor Components LLC, 2009. 1 Apr. 2009. <http://onsemi.com>
34. "THT/SMT Power Inductors: Toroid-Designed for National's 260 kHz Simple Switcher." Pulse, 2006. 1 Apr. 2009. <www.pulseeng.com>
35. "Schottky Rectifiers." STMicroelectronics, 2002. 1 Apr. 2009. <http://www.st.com>
36. MIL-HDBK-340A: Department of Defense Handbook Test Requirements for Launch, Upper-Stage, and Space Vehicles Vol I: Baselines. Defense Standardization Program Office (DLSC-LM): Los Angeles, 1999.
37. Ibid
38. Ibid
39. Ibid
40. Rigmaiden, David. Interview. Naval Postgraduate School, Monterey. 1 Apr. 2009.
41. Coelho, Roland. Teleconference. Naval Postgraduate School, Monterey. 1 Apr. 2009.
42. Rigmaiden, David. Interview. Naval Postgraduate School, Monterey. 1 Apr. 2009.
43. "Maxim 12-Bit +Sign Digital Temperature Sensors with Serial Interface." Maxim Integrated Products: Sunnyvale, 2005
44. Phelps, Ron. Interview. Naval Postgraduate School, Monterey. 1 May 2009.
45. Ibid
46. Ibid
47. Rigmaiden, David. Interview. Naval Postgraduate School, Monterey. 1 Apr. 2009.
48. Ibid
49. Ibid

INITIAL DISTRIBUTION LIST

1. Defense Technical Information Center
   Ft. Belvoir, Virginia

2. Dudley Knox Library
   Naval Postgraduate School
   Monterey, California

3. James H. Newman, Ph.D.
   Naval Postgraduate School
   Monterey, California